# MZ-R30
OPERATION MANUAL

Table. 2-1 Comparison of 3rd Generation and 4th Generation Recording/Playback Units

Unit Functions	MZ-B3	MZ-R3	MZ-R30
Play VOLUME	Rotation mechanism	Electronic VOL	Electronic VOL
Remote control	✕	○	○
Headphone output	○	○	○
Line output	✕	○	○
Digital output	✕	✕	✕
Line input	✕	○	○
Digital input	✕	○	○
Microphone input	○ (Built-in:Monaural External:Stereo)	○ (External:Stereo)	○ (External:Stereo)
AVLS	✕	○	○
DBB (Digital bass boost)	✕	○	○
RESUME	○ (Always ON)	○ (Always ON)	○ (Always ON)
Beep	✕	○	○
Recording method	AGC only	AGC or manual	AGC or manual
Synchro-recording	✕	✕	◎
Monaural recording	○ Analogue : (L-ch + R-ch) /2 Digital : L-ch only	○ Analogue : (L-ch + R-ch) /2 Digital : L-ch only	◎ Analogue : (L-ch + R-ch) /2 Digital : (L-ch + R-ch) /2
Monaural playback	○	○	○
Automatic track mark	✕	○	○
Fast forward playback	○	✕	✕
Track search	✕	✕	◎
Character input	✕	○	○
Built-in sampling rate converter	✕	✕	◎ (32, 44.1, 48 [kHz])

Note: ◎ in the table indicates a new function.

Table. 3-1 Main ICs Used

| Circuit block / Corresponding model	1st Generation MZ-1	2nd Generation MZ-R2	3rd Generation MZ-R3, B3	4th Generation MZ-R30
ATRAC encoder/decoder	CXD2527R (x2)	CXD2531AR	CXD2536R	CXD2652R
Shock proof Memory controller	CXD2526Q	CXD2526AR	CXD2536R	CXD2652R
EFM ACIRC Encoder/decoder	CXD2525R	CXD2525R	CXD2535BR	CXD2652R
ADIP Demodulator	CXA1380N	CXA1380N	CXD2535BR	CXD2652R
Servo Signal processor	CXA1602R	CXA1602R	CXD2535BR	CXD2652R
RF amplifier	CXA1381R	CXA1861R	CXA1981AR	CXA2523R
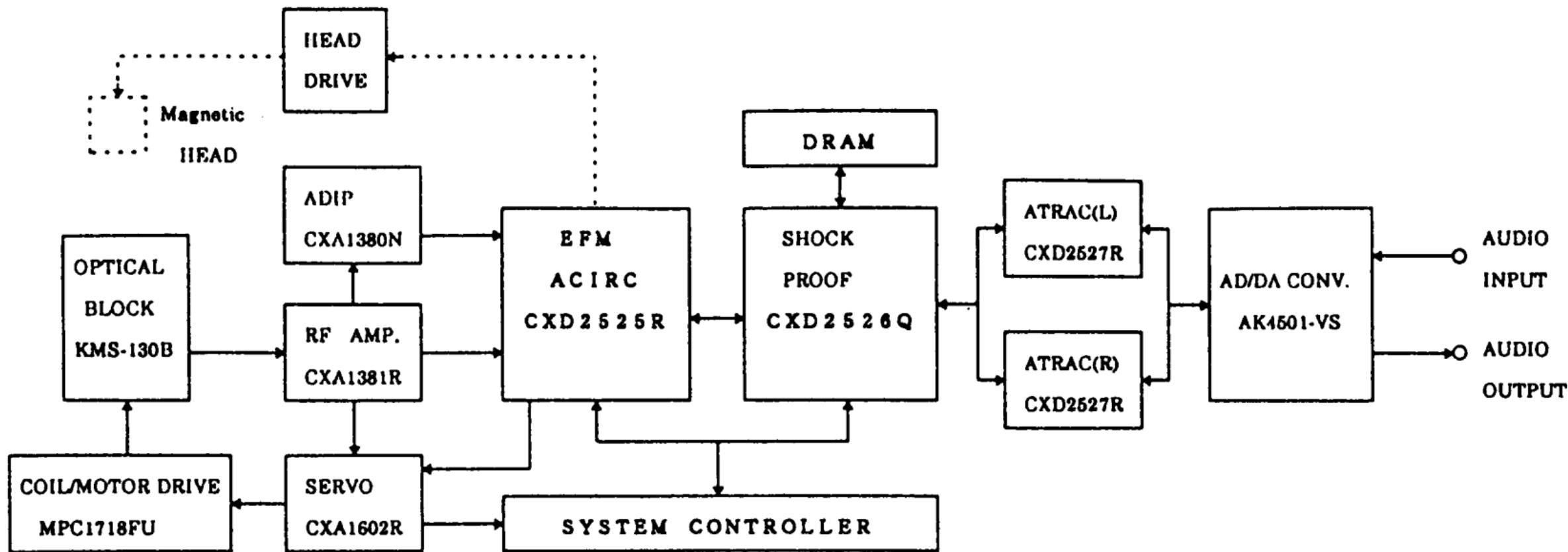
Fig. 3-1 1st Generation Mini Disc System
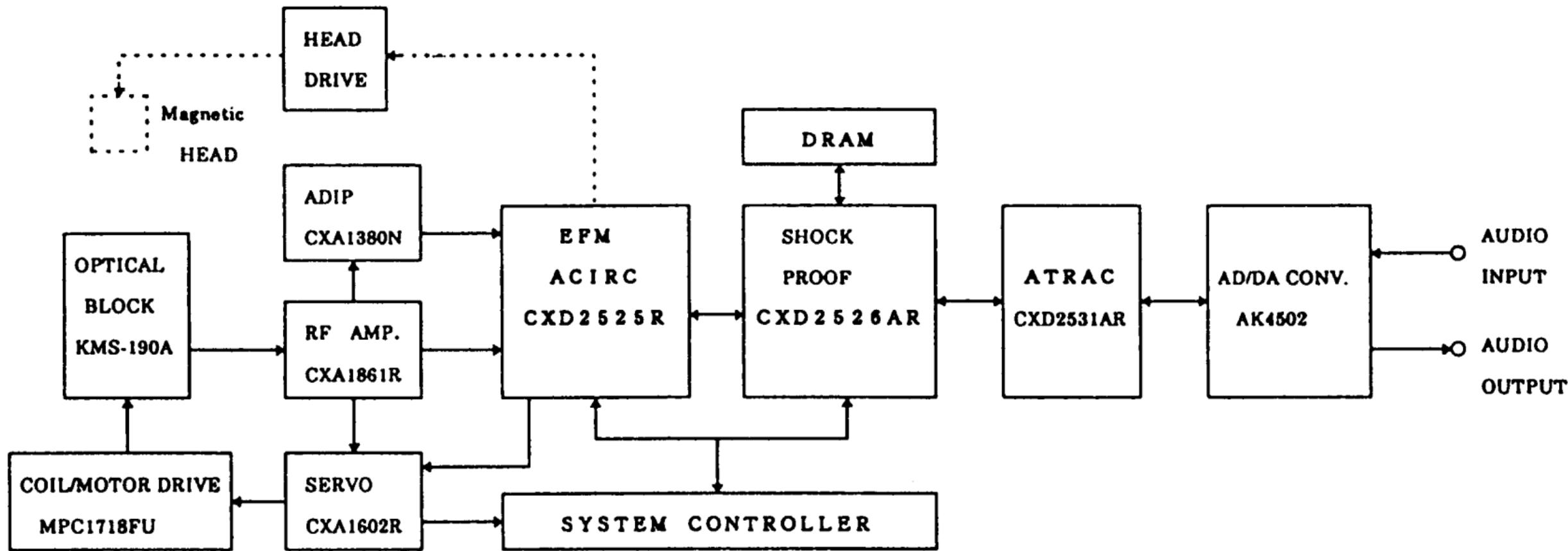
**Fig. 3-2 2nd Generation Mini Disc System**
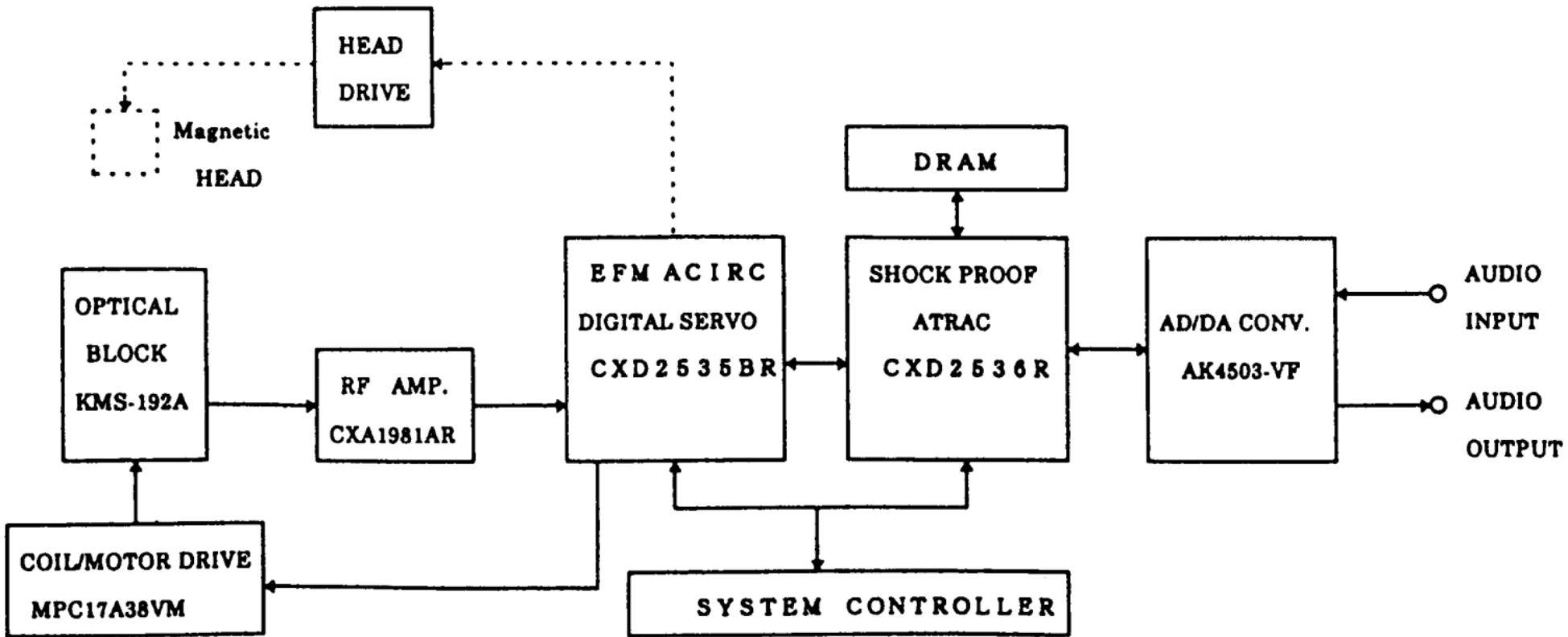
Fig. 3-3 3rd Generation Mini Disc System
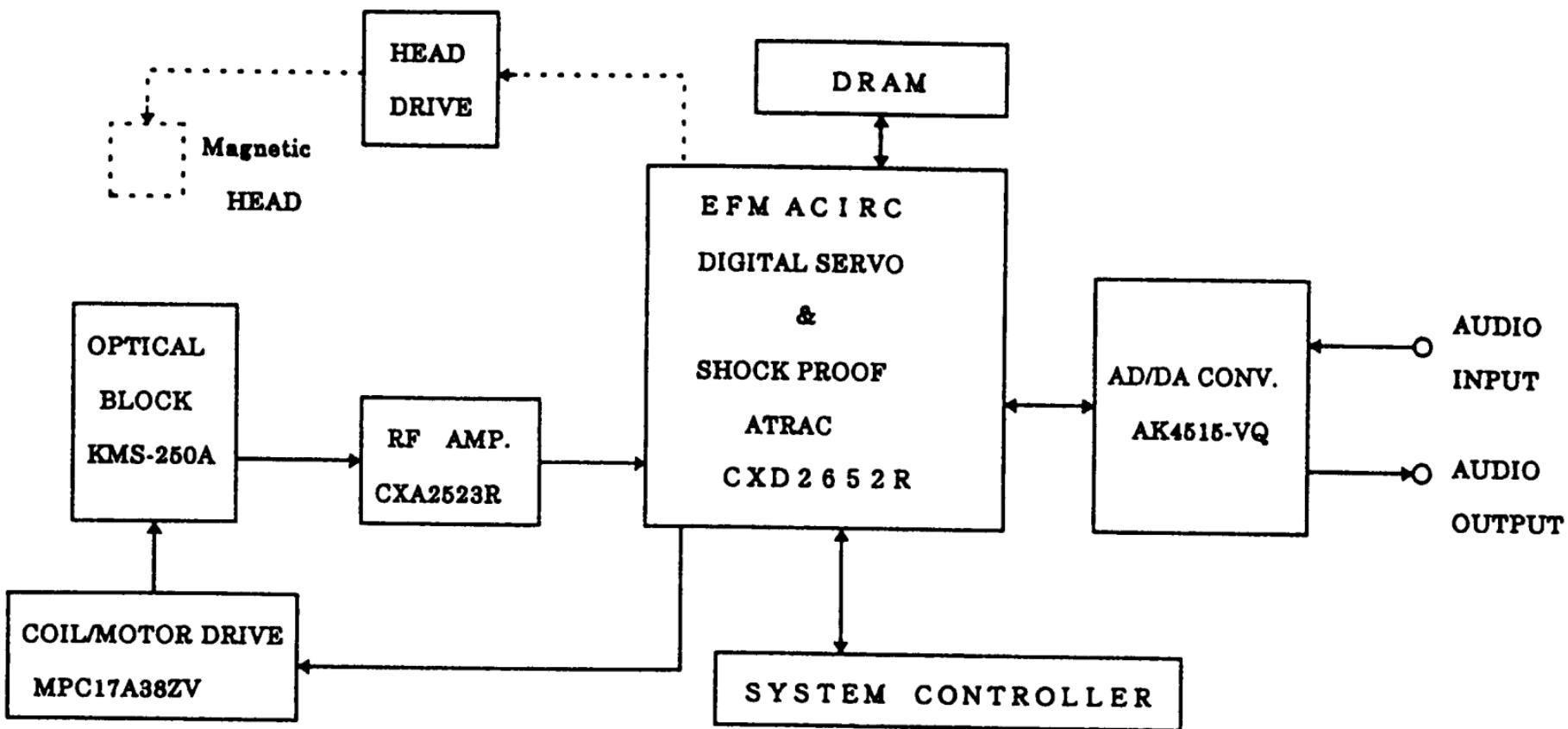
Fig. 3-4 4th Generation Mini Disc System

IC506
REC DRIVE

EFM SIGNAL

MAGNETIC HEAD

FROM IC801

IC509
4M DRAM

DIGITAL IN

IC302
MIC AMP

OPTICAL PICK-UP

IC501
RF AMP
· ERROR AMP
· APC CIRCUIT

EFM SIGNAL

ERROR SIGNAL

IC503
DIGITAL SIGNAL PROCESSOR
· ATRAC ENCODER/DECODER
· RAM CONTROLLER
· ACIRC ENCODER/DECODER
· EFM MODURATOR/DEMODURATOR
· SAMPLING RATE CONVERTER
· DIGITAL SERVO PROCESSOR

DIGITAL DATA

IC303
AD/DA CONVERTER
· AD CONVERTER
· DA CONVERTER
· DIGITAL FILTER
· DBB
· INPUT SELECTOR

L/R

L/R

MIC IN

L/R

LINE IN

AD DATA

DA DATA

FOCUS/TRACKING SERVO COIL

IC505
COIL/MOTOR DRIVE

SERVO SIGNAL

SLED/SPINDLE MOTOR

IC304
BUFFER

L/R

IC352
AUDIO GAIN CONTROL

L/R

IC805
H. P. AMP

L/R

L/R

HEAD PHONE

CONTROL SIGNAL

CONTROL SIGNAL

LINE OUT

L/R

IC801
SYSTEM CONTROLLER
· CONTROL THE WHOLE SYSTEM
· LCD DRIVER
· CONTROL THE DSP IC503
· CONTROL THE AD/DA CONV. IC303
· CONTROL THE REC DRIVE IC506
· CONTROL THE NV RAM IC807
· CONTROL THE STEPPING
        MOTOR DRIVE IC702

TO IC506

CONTROL SIGNAL

CONTROL SIGNAL

STEPPING MOTOR

IC702
STEPPING MOTOR DRIVE

CONTROL SIGNAL

IC804
REAL TIME CLOCK

IC807
NV RAM

IC803
TEMP METER

JOG

KEY & SWITCH

LCD

Fig. 4-2 Microprocessor Interface

5-1. Types of Power Supply

This unit can operate on the following four types of power supplies.

- AC adapter (AC-MZ60) ... 6.0 [V] (Accessory)
- Rechargeable lithium ion battery (LIP-12 (H)) ... 3.6 [V] (Accessory)
- Dry battery (SIZE "AA" dry battery x 2) ... 3.0 [V] (Optional)
- Rechargeable nickel hydrogen battery (BP-DM20) ... 2.4 [V] (Optional)

Table. 5-1 shows how long the respective batteries will last in continued use.
As shown in **Table. 5-1**, compared to MZ-R3, batteries can last twice longer according to how they are combined.

Table. 5-1 Comparison of Durability of Batteries (MZ-R3, MZ-R30)

No.	Battery	MZ-R3		MZ-R30	
		During Recording	**During Playback**	**During Recording**	**During Playback**
1.	Rechargeable lithium ion battery (LIP-12 (H))	Approx. 2.5 hours	Approx. 4 hours	Approx. 5 hours	Approx. 8 hours
2.	SONY alkaline dry battery (LR6 (SG)x2)	Approx. 2 hours	Approx. 4 hours	Approx. 3 hours	Approx. 6.5 hours
3.	Rechargeable nickel hydrogen battery (BP-DM20)	Approx. 2 hours	Approx. 3 hours	Approx. 3 hours	Approx. 4.5 hours
4.	1+2	Approx. 4.5 hours	Approx. 8 hours	Approx. 8.5 hours	Approx. 15 hours
5.	1+3	Approx. 4.5 hours	Approx. 7 hours	Approx. 8.5 hours	Approx. 14.5 hours

5-2. Differentiation of Power Supply

The system controller IC801 when started, will immediately determine where the power supply voltage is being supplied from. The unit must be stopped if AC adapter and batteries outside the specification are used.
The system controller IC determines the source of power supply from the following three detection results.

(1) Pin �59 [UNMNT] : Voltage obtained by resistance-dividing the voltage of the plus side of the power supply (UNREG voltage)
(2) Pin �===60 [LIMNT (LI+MNT)] : Voltage obtained by resistance-dividing the lithium ion battery voltage
(3) Pin ㊝53 [AM3] : Voltage obtained by resistance-dividing the nickel hydrogen battery voltage or the dry battery voltage.

Table. 5-2 List for Differentiating the Power Supply

|	Pin �59 [UNMNT]	Pin ㊝60 [LIMNT (LI+MNT)]	Pin ㊝53 [AM3]
During DC drive	H	L	L
During rechargeable lithium ion battery drive	H	H	L
During rechargeable nickel hydrogen battery drive	H	L	H
During alkaline AA dry battery drive	H	L	H

5-3. Circuit Voltage
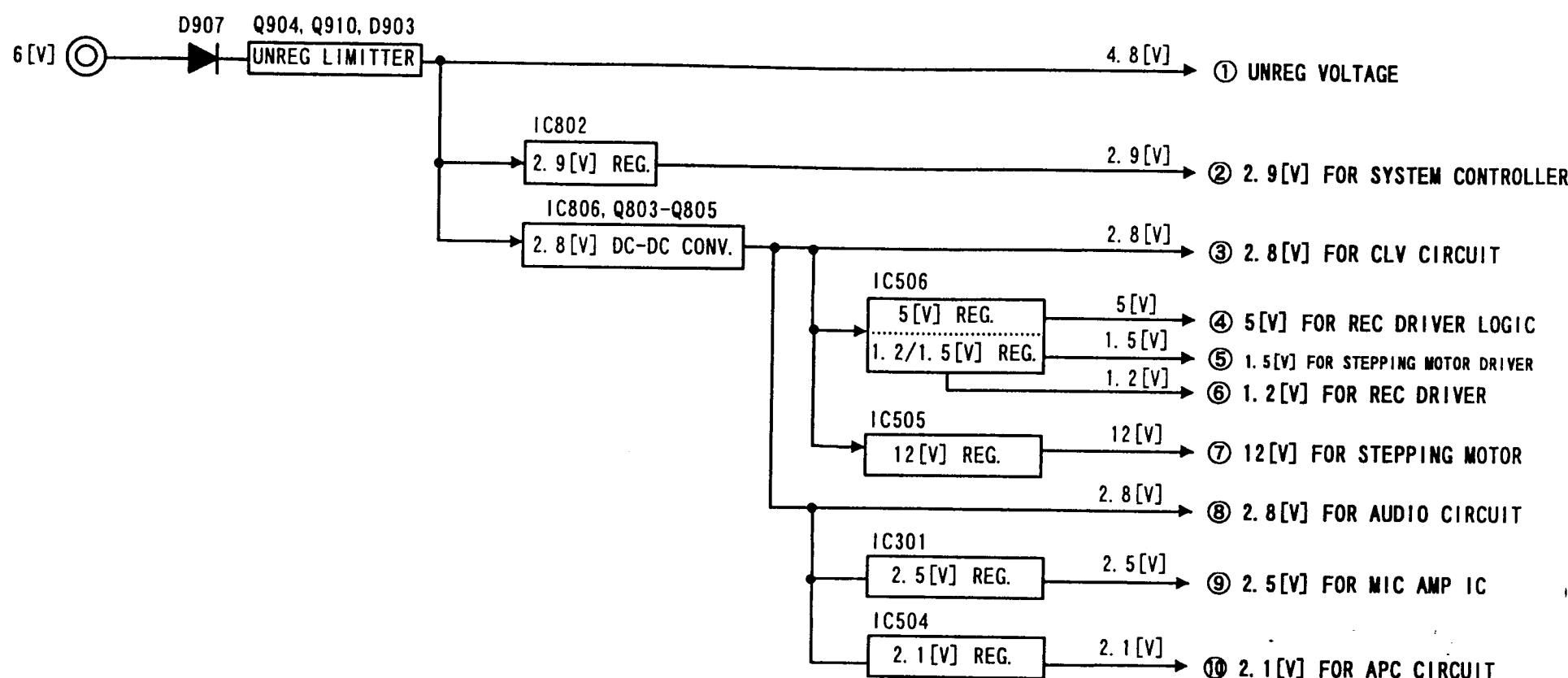
Fig. 5-1 Generation Voltage Block Diagram

The voltages generated by this unit during DC drive are as follows. (See **Fig. 5-1**.)

① **UNREG voltage → [Q904, Q910, D903]**
  - This UNREG voltage 4.8 [V] is generated from the 6[V] of the AC adapter.
  - Serves as the driver power supply of the coil/motor drive IC505.

② **MICON +B voltage → [RESET IC802]**
  - 2.9 [V] serving as the voltage for driving the system controller IC801.

③ **CLV circuit voltage → [2.8 [V] DC-DC converter (IC806, Q803-Q805)]**
  - 2.8 [V] serving as the voltage used by the CLV circuit (RF amplifier IC501, DSP IC503, coil/motor drive IC505, etc.).

④ **REC driver logic voltage → [5[V] REG. (IC506)]**
  - 5.0 [V] serving as the voltage for driving the internal logic circuit of the REC driver IC506.

⑤ **Stepping motor driver voltage → [1.2/1.5[V] REG. (IC506)]**
  - 1.5 [V] serving as the H bridge power supply voltage of the stepping motor.

⑥ **REC driver voltage → [1.2/1.5[V] REG. (IC506)]**
  - 1.2 [V] serving as the power supply voltage of the overwrite head driver during recording.

⑦ **Stepping motor voltage → [12]V] REG. (IC505)]**
  - 12 [V] serving as the voltage for the predriver power supply circuit inside IC505.
  - 12 [V] serving as the voltage for driving the stepping motor.

⑧ **AUDIO circuit voltage → [2.8[V] DC-DC converter (IC806, Q803-Q805)]**
  - 2.8[V] used by the audio circuit (AD/DA converter IC303, audio gain control IC352, etc.)

⑨ **MIC AMP IC voltage → [2.5 [V] REG. (IC301)]**
  - 2.5 [V] serving as the voltage for driving the MIC amplifier IC302.

⑩ **APC circuit voltage → [2.1 [V] REG. (IC504)]**
  - 2.1 [V] serving as the voltage used by the APC circuit during recording.

3. Generation of APC circuit voltage
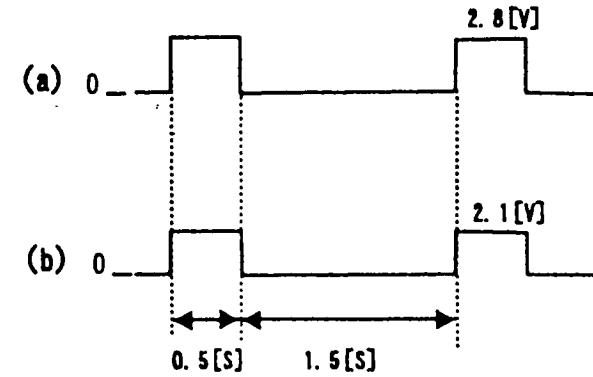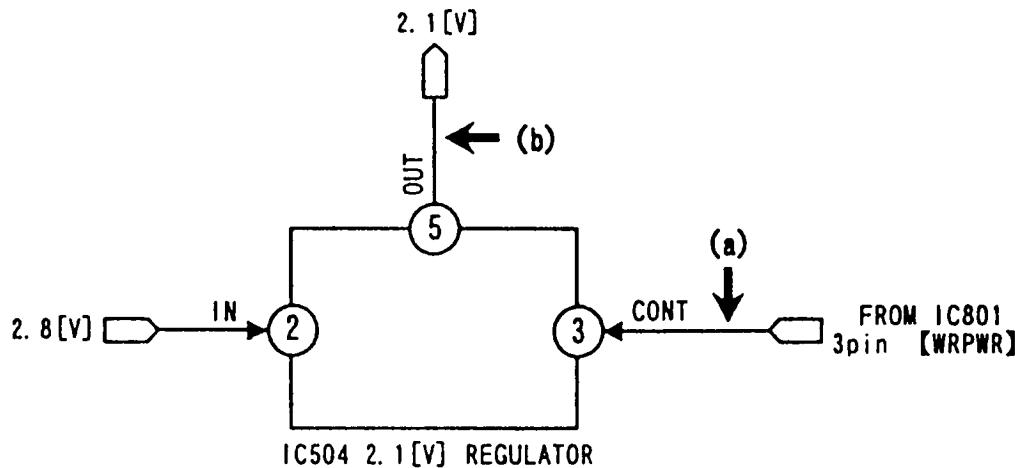
Fig. 5-2 2.1 [V] Regulator

Fig. 5-2 shows the 2.1 [V] regulator IC504. As shown in the figure, when 2.8 [V] is input to Pin ② [IN] of IC504, IC504 is started. When IC504 is started, 2.1 [V] is generated by the internal series regulator. This voltage is then synchronized with the "H" period of the laser power switching signal from Pin ③ [WRPWR] of the system controller IC801 input to Pin ③, and output from Pin ⑤ [OUT].

4. Generation of the CLV circuit voltage and the voltage for Audio circuit
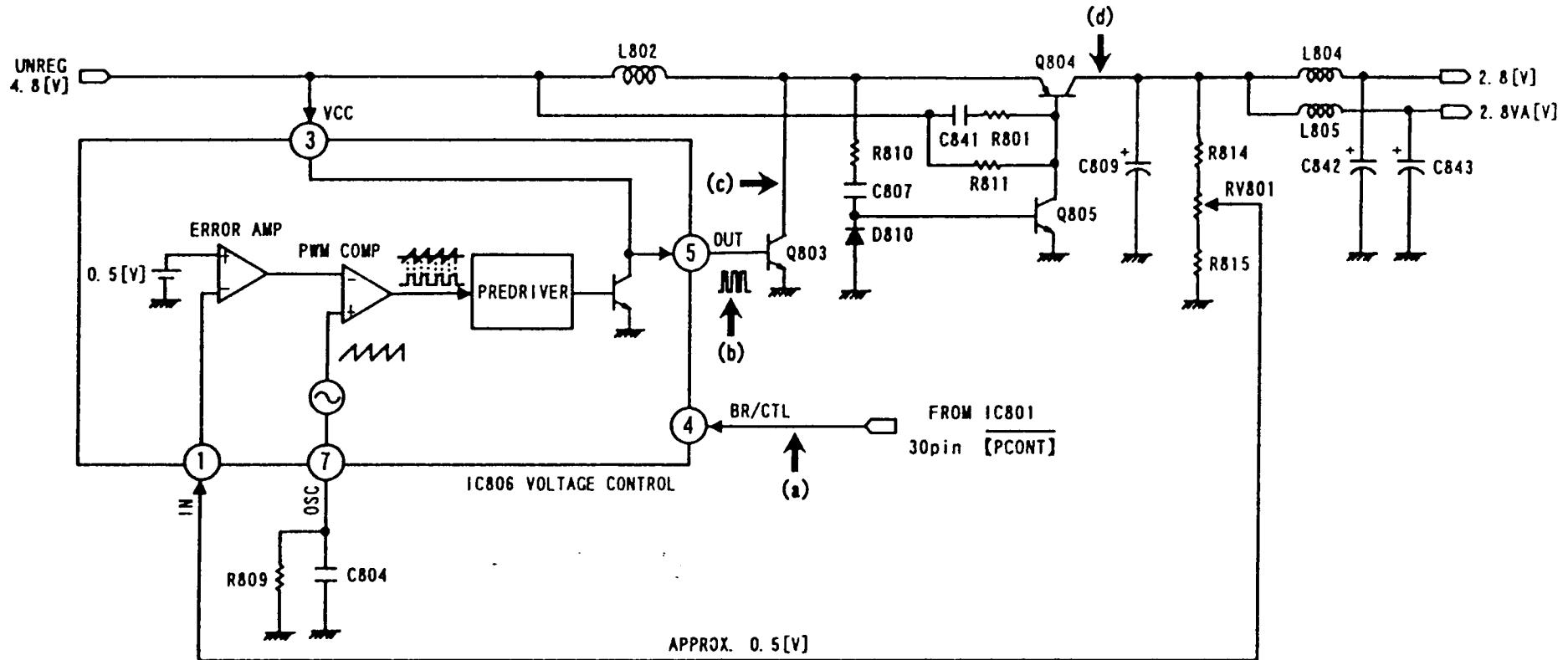
Fig. 5-3 2.8 [V] DC-DC converter circuit

Fig. 5-4 shows the (a) to (d) waveforms of **Fig. 5-3**.
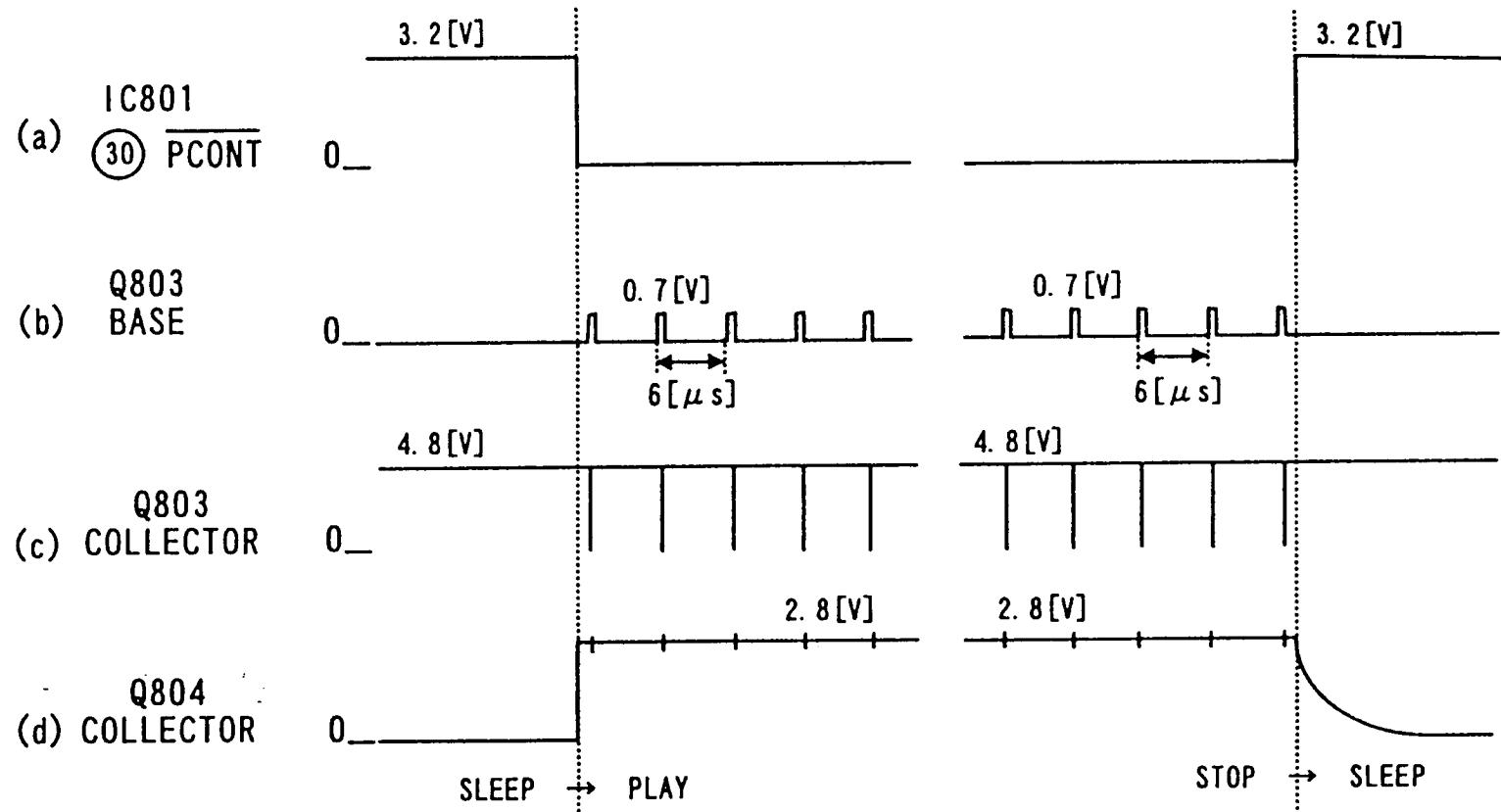
Fig. 5-4 Waveform Timing Diagram (During Battery Drive)
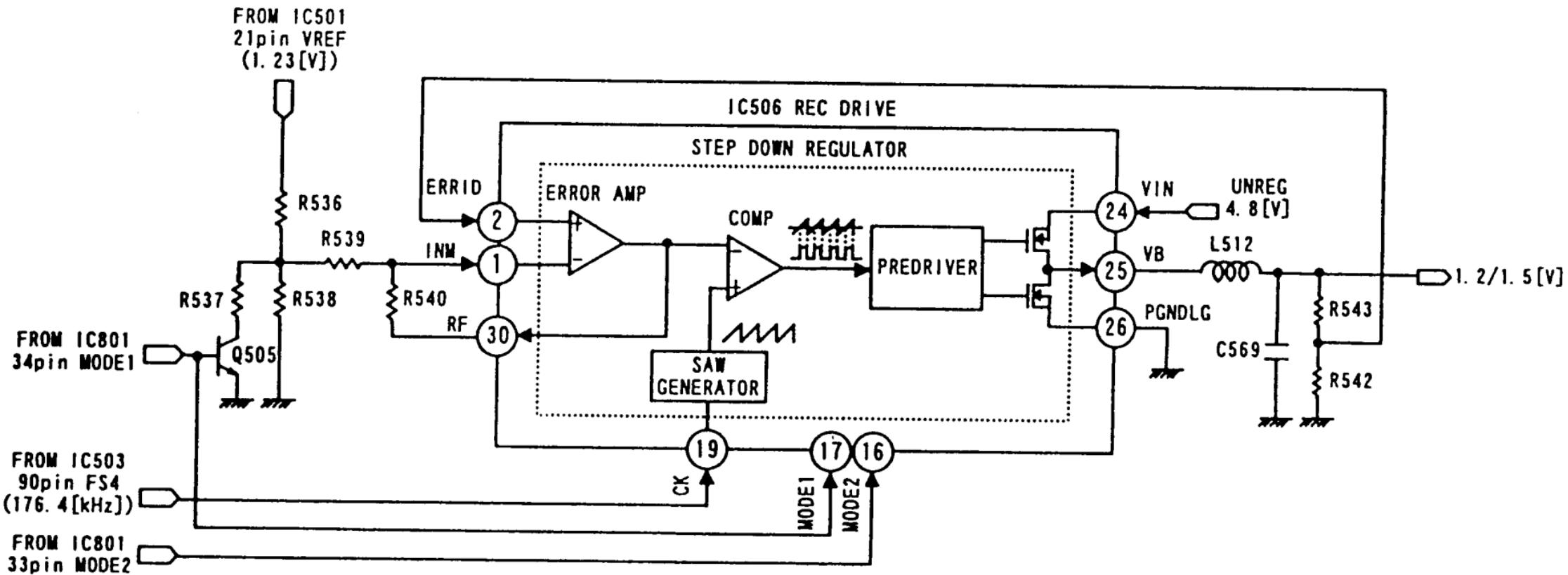
Fig. 5-5 1.2/1.5 [V] Regulator Block Diagram

Table. 5-3 List of IC506 Mode Settings

MODE1	MODE2	STEP UP REG	STEP DOWN REG	EFM Logic Section	Operation Mode
H	H	STOP	STOP	STOP	During stop and playback
L	H	POWER ON	STOP	STOP	Not used
L	L	POWER ON	POWER ON 1.5 [V] output	STOP	During stepping motor operation
H	L	POWER ON	POWER ON 1.2 [V] output	POWER ON	During recording

7. Generation of Stepping Motor Voltage
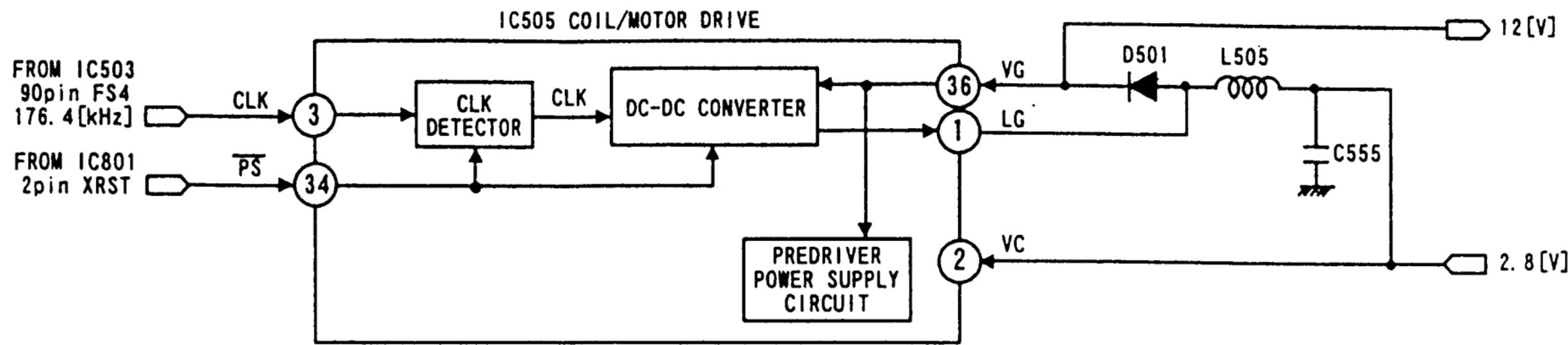
Fig. 5-6 12 [V] DC-DC CONVERTER Block Diagram
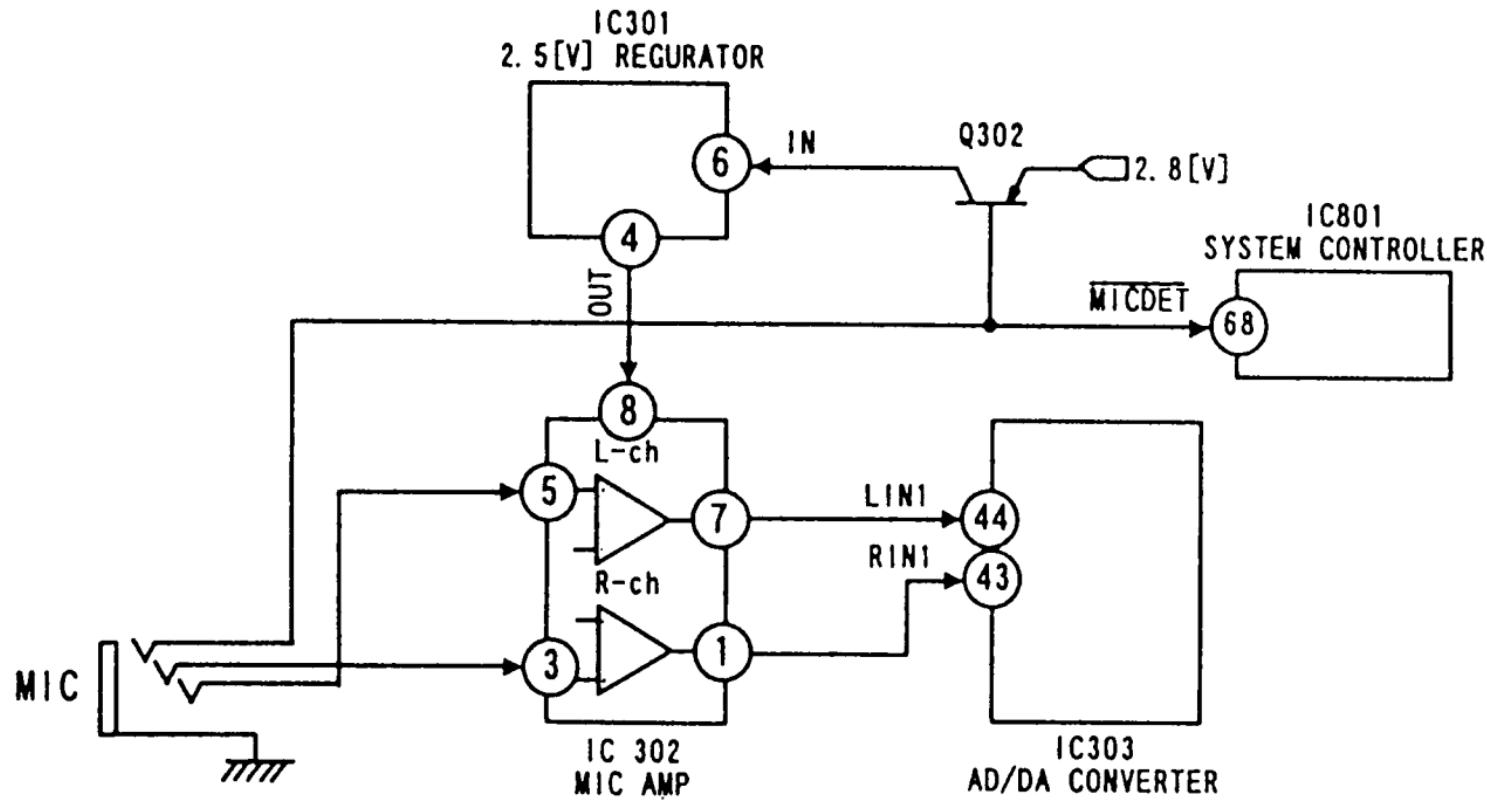
Fig. 5-7 Generation of MIC AMP IC302 Drive Voltage
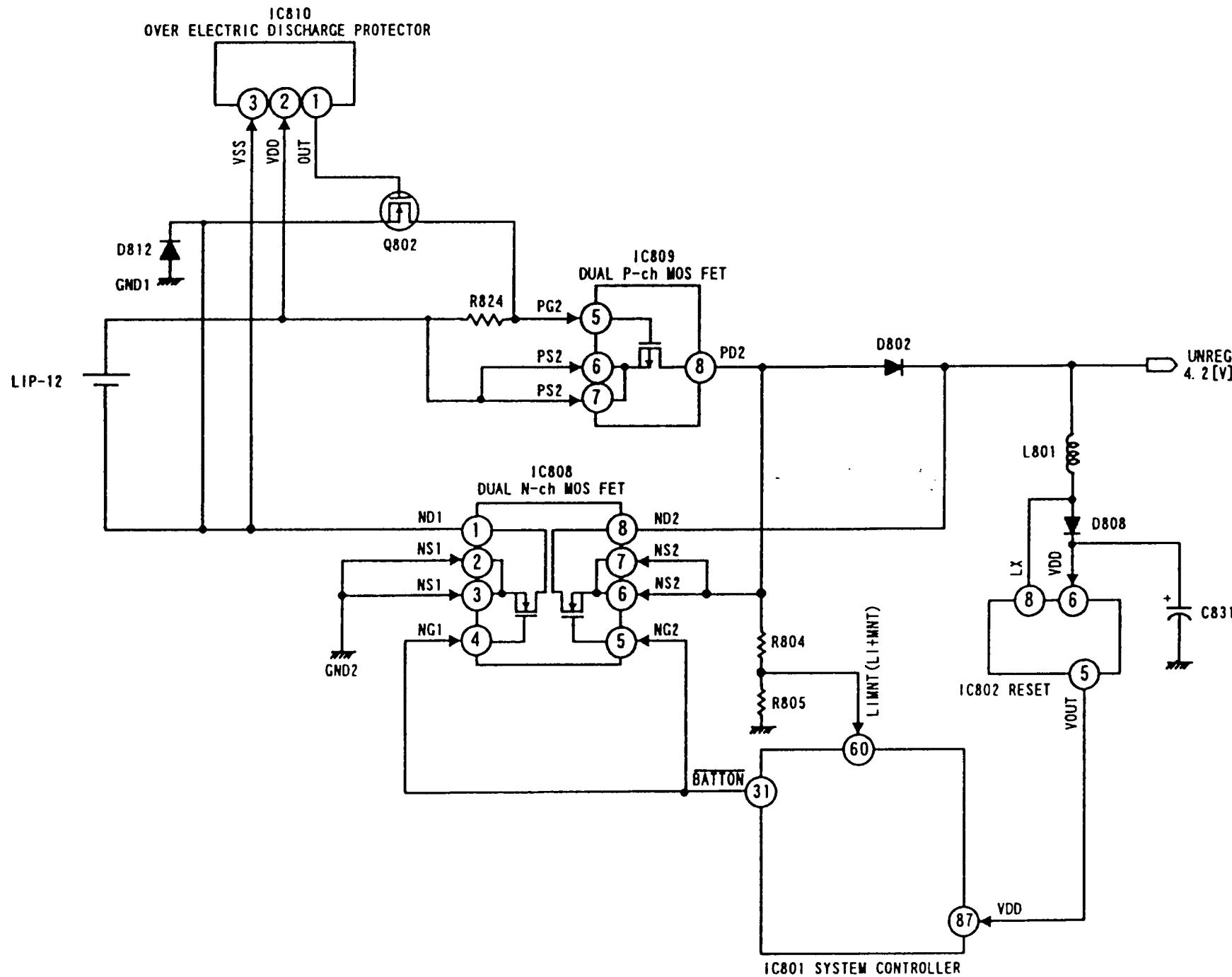
Fig. 5-8 Power Supply Circuit when Driving with Rechargeable Lithium Ion Battery
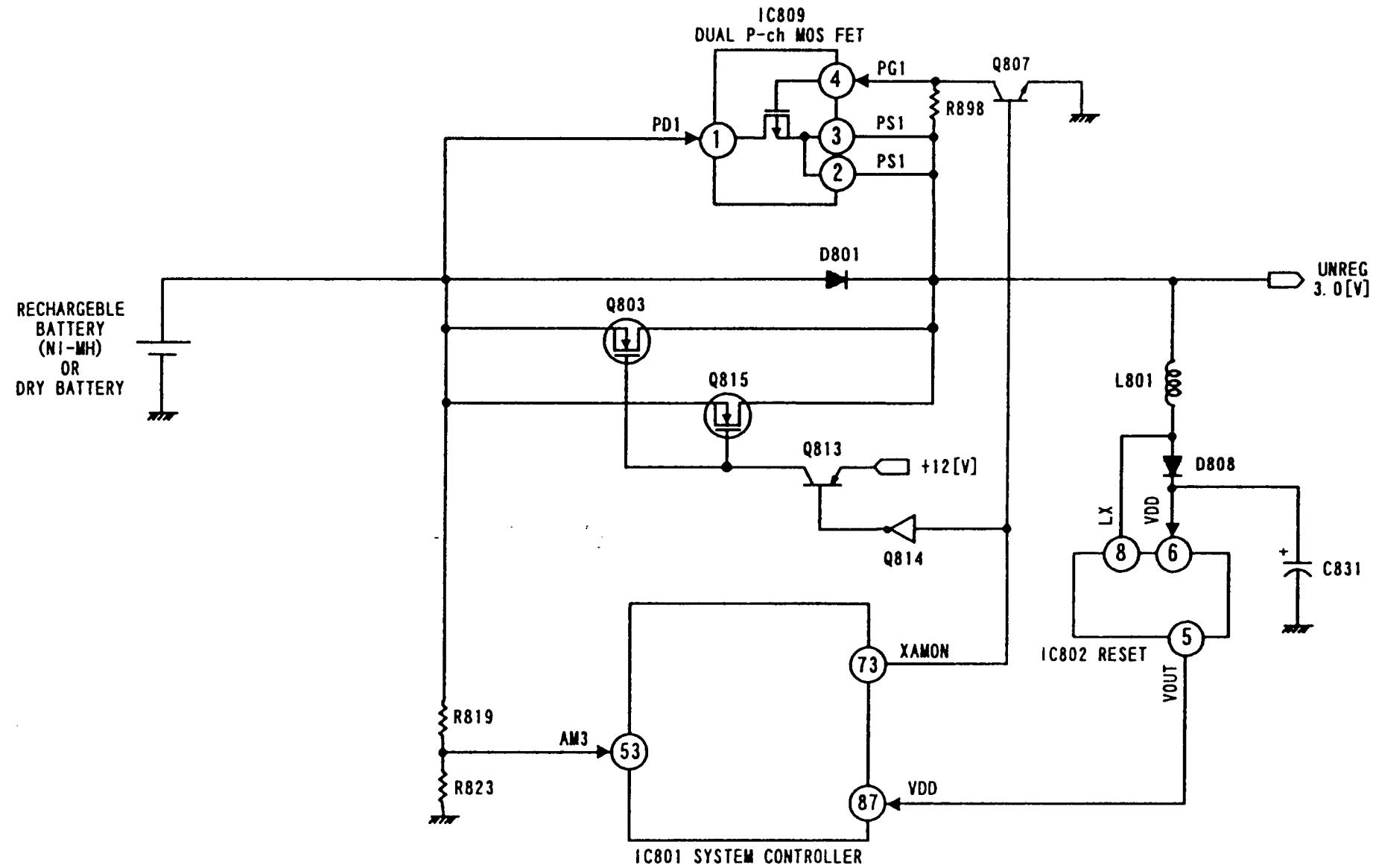
Fig. 5-9 Power Supply Circuit When Driving with External Battery

5-6. Operations During Charging
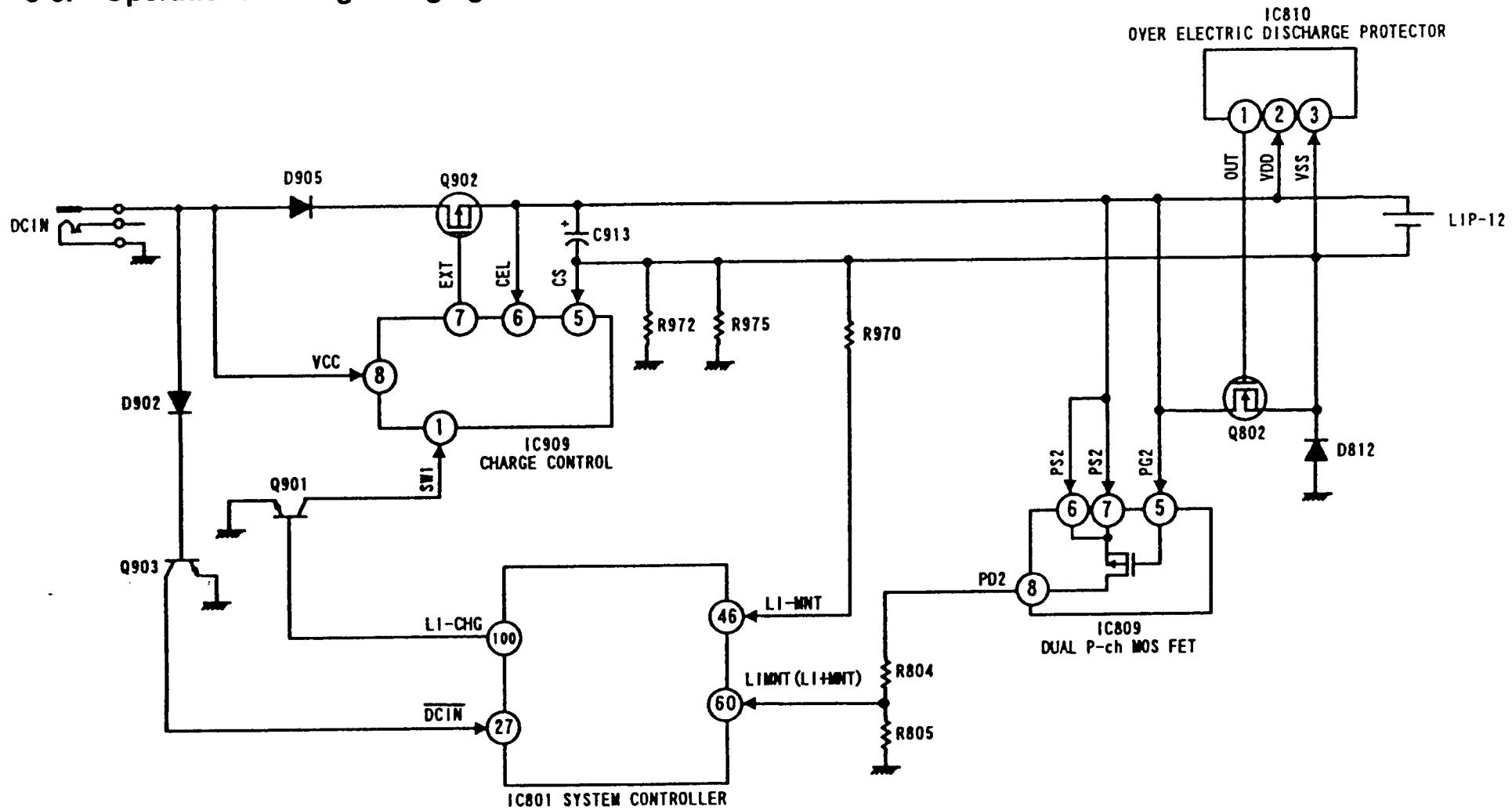
Fig. 5-10 Operations During Charging
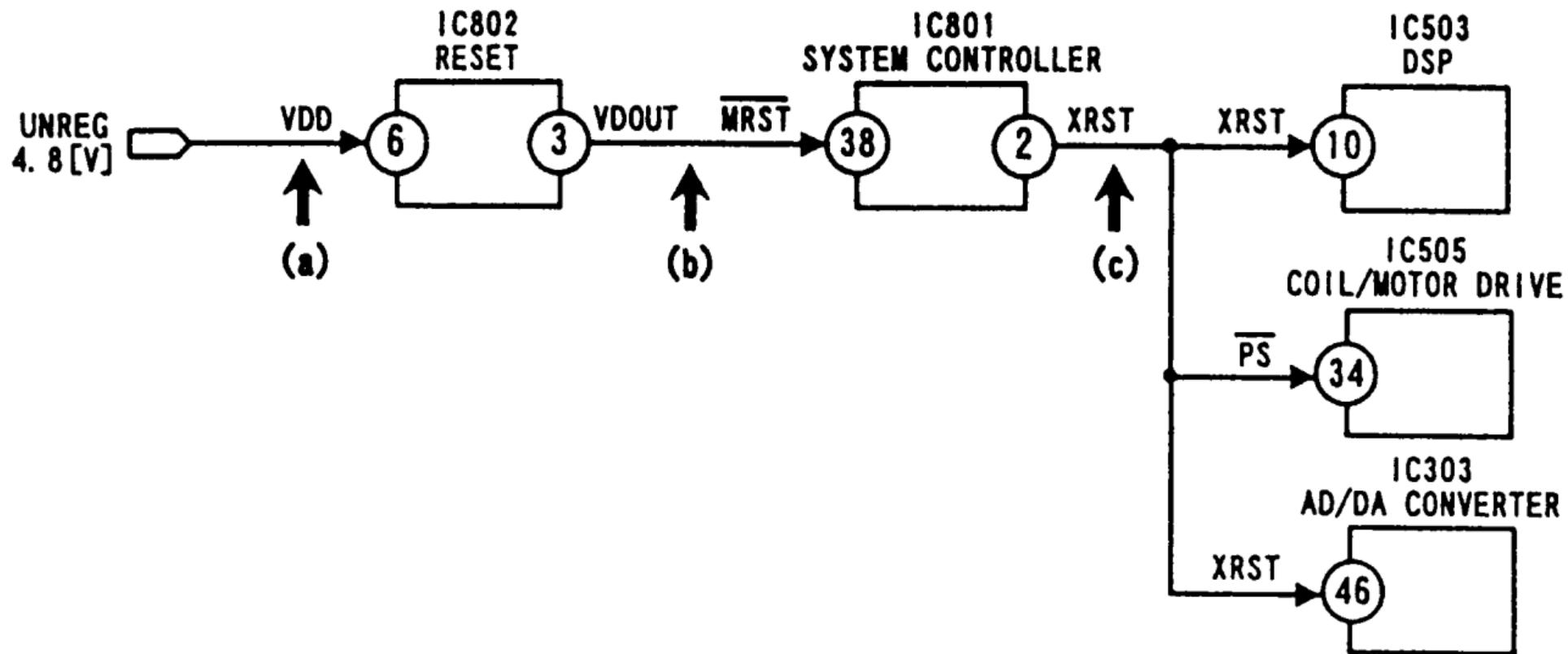
Fig. 5-11 Reset Circuit

(a)

4. 8 [V]

0

(b)

2. 9 [V]

0

(c)

2. 9 [V]

0

230 [ms]
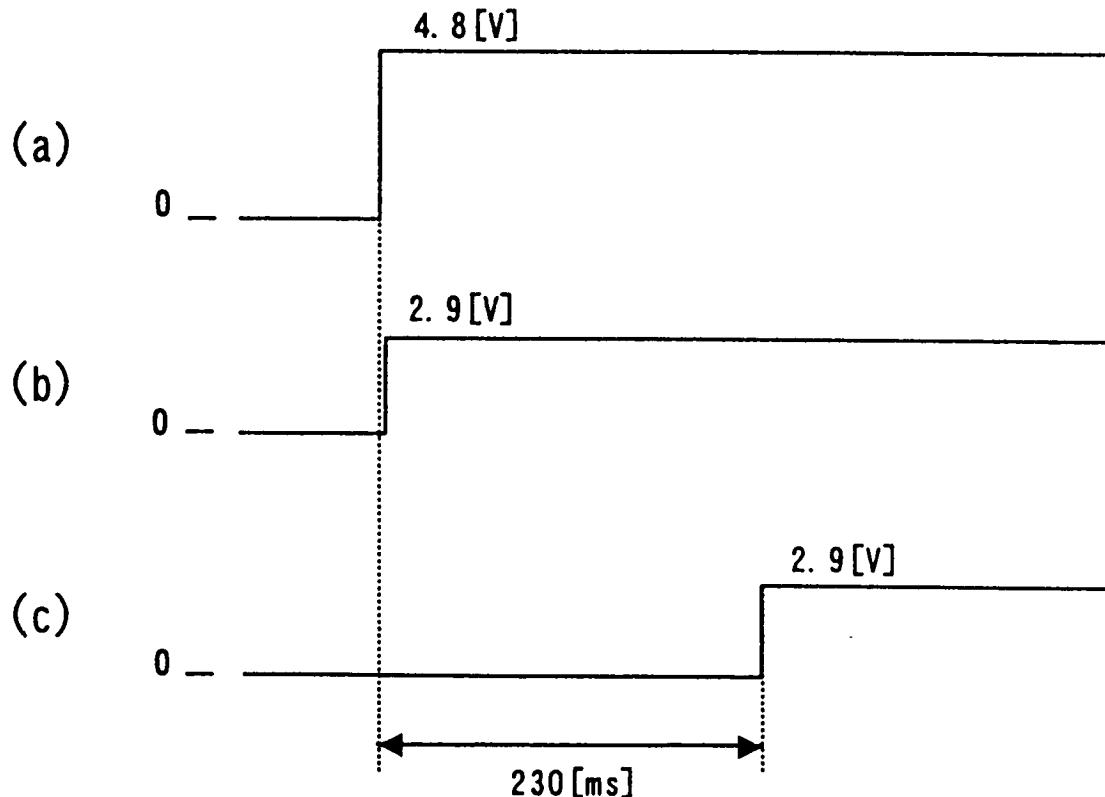
Fig. 5-12 Timing of Reset Signals
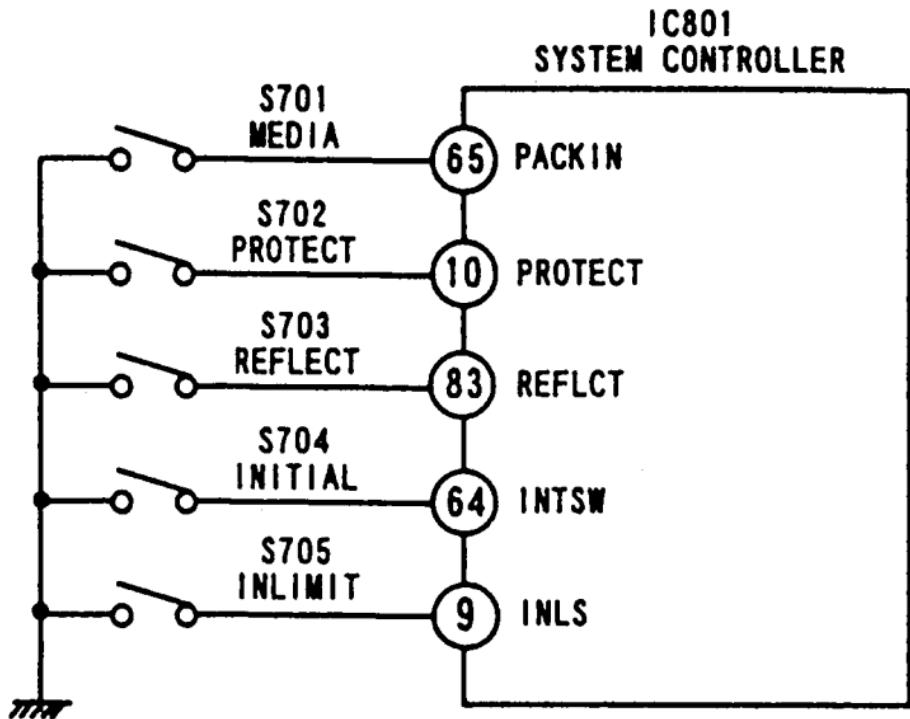
Fig. 6-1 Detection Switches of Mechanism

Table. 6-1 Detection Switches of Mechanism Section

Switch No.	Switch Name	System Controller IC Detection Terminal	Details of Detection
S701	MEDIA	Pin ⑥⑤ [PACKIN]	Determines whether a disc is loaded (Loaded: "L", Not loaded: "H")
S702	PROTECT	Pin ⑩ [PROTECT]	Determines the rec-proof state by the PROTECT detection hole of the disc (When PROTECT : "H")
S703	REFLECT	Pin ⑧③ [REFLCT]	Determines the reflectance by the MO detection hole of the disc to determine if CD or MO (When CD: "L". When MO: "H")
S704	INITIAL	Pin ⑥④ [INTSW]	Detects the eject mode
S705	INLIMIT	Pin ⑨ [INLS]	Detects the completion of movement of the optical block to the innermost circumference

Table 6-2. Discrimination of Input Source

	MICDET (Pin ㊽)	OPTDET (Pin ㊼)	JACKDET (Pin ㊻)
MIC IN jack detection	L	H	H
DIGITAL IN jack detection	H	H	L
LINE IN jack detection	H	L	L
Not connected	H	H	H

When several input sources are connected, they are used in the following priority order.

      1. DIGITAL IN
      2. MIC IN
      3. LINE IN

Table. 6-3 Timing during Recording

| MODE1	MODE2	EFM signal	HA	HB
H	L	L	L	H
H	L	H	H	L
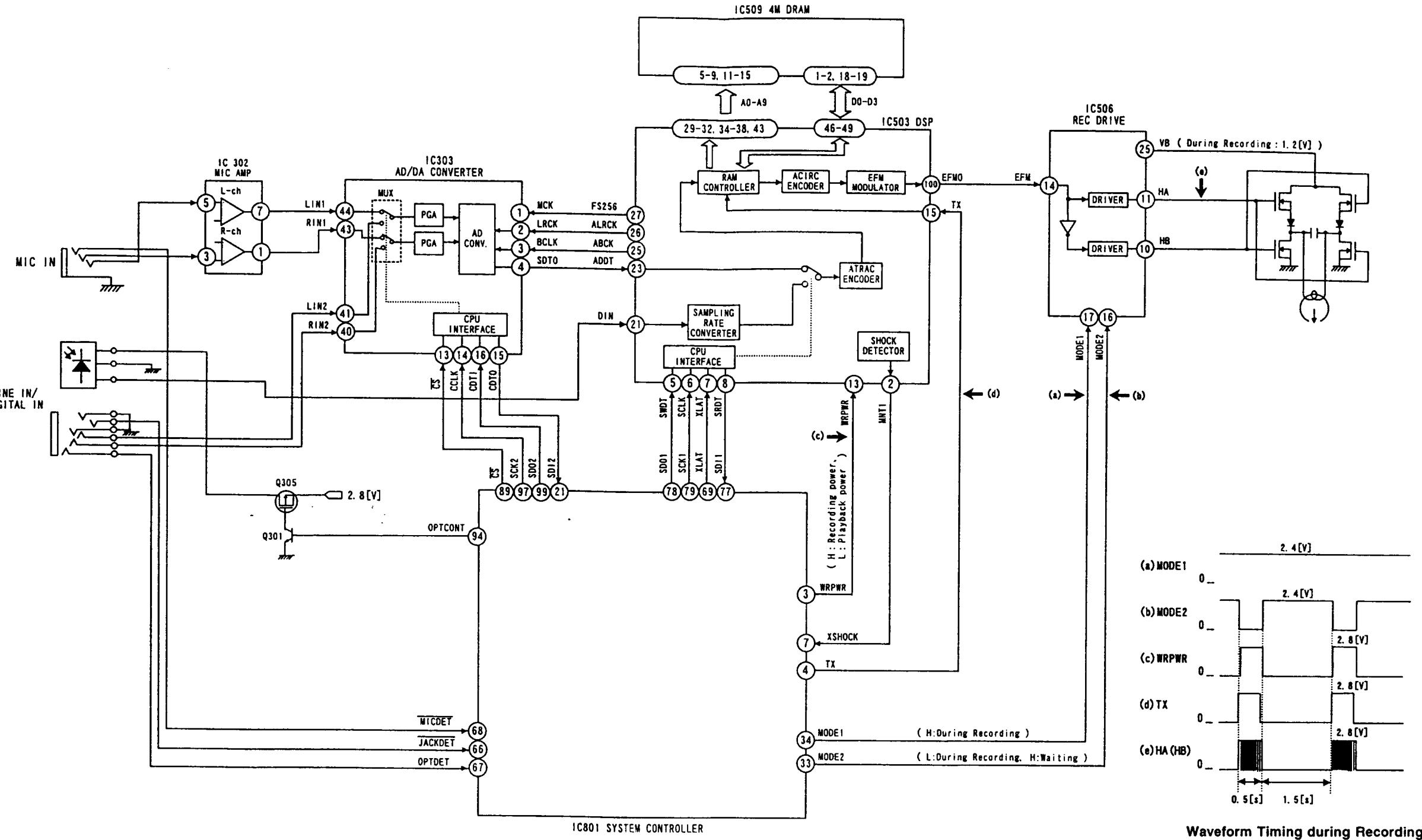
Fig. 6-2 Block Diagram of the Signal Circuit during Recording

7. Monitor output
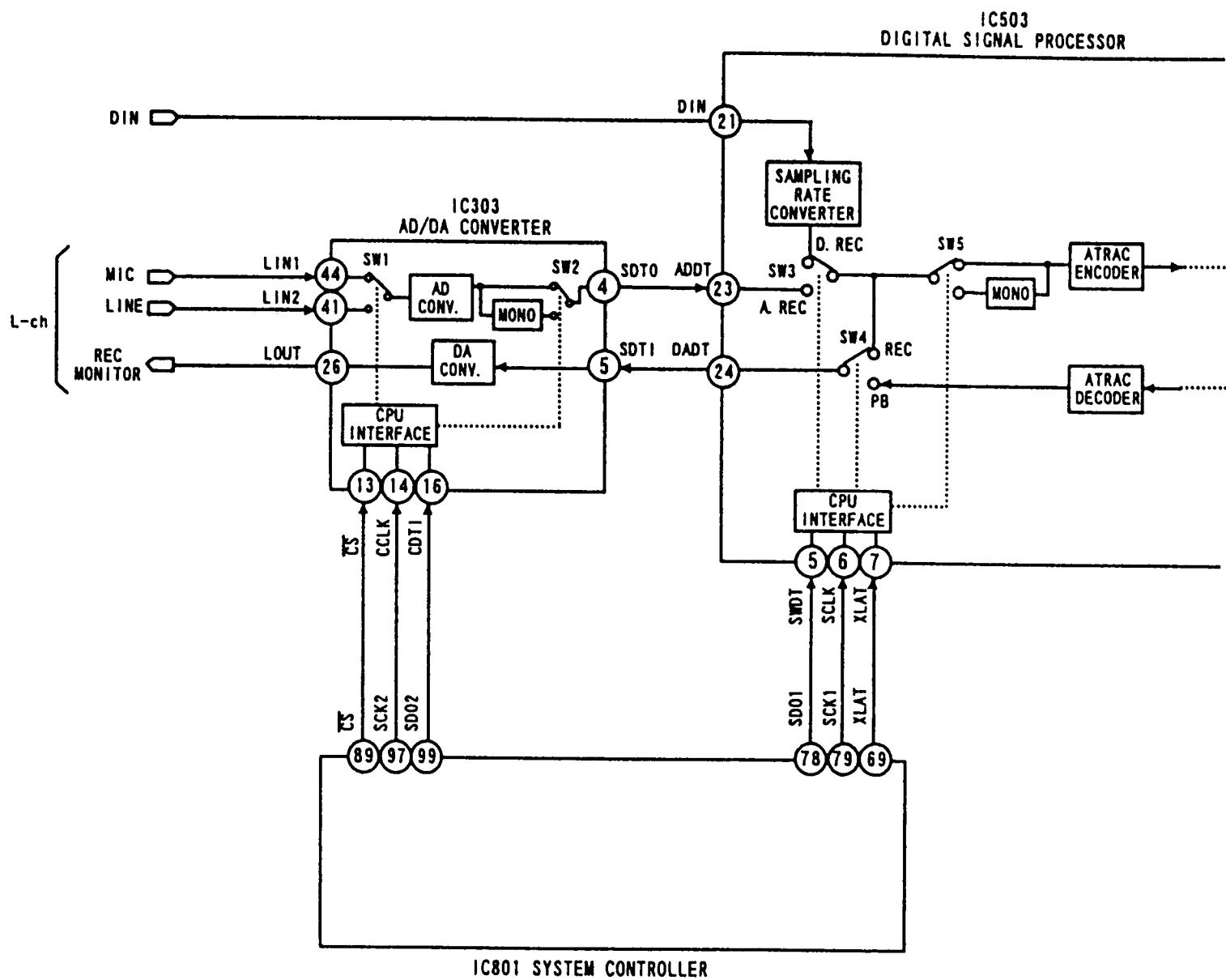
Fig. 6-3 Monitor Output During Recording

Table. 6-4 Connection of Internal Switches During Recording

	SW1	SW2	SW3	SW4	SW5	Monitor output
ANALOG recording (Stereo)	MIC/LINE	STEREO	A. REC	REC	STEREO	STEREO
ANALOG recording (Monaural)	MIC/LINE	MONAURAL	A. REC	REC	STEREO	MONAURAL
DIGITAL recording (Stereo)	———	———	D. REC	REC	STEREO	STEREO
DIGITAL recording (Monaural)	———	———	D. REC	REC	MONAUAL	STEREO

Fig. 6-4 Block Diagram of the Signal Circuit during Playback
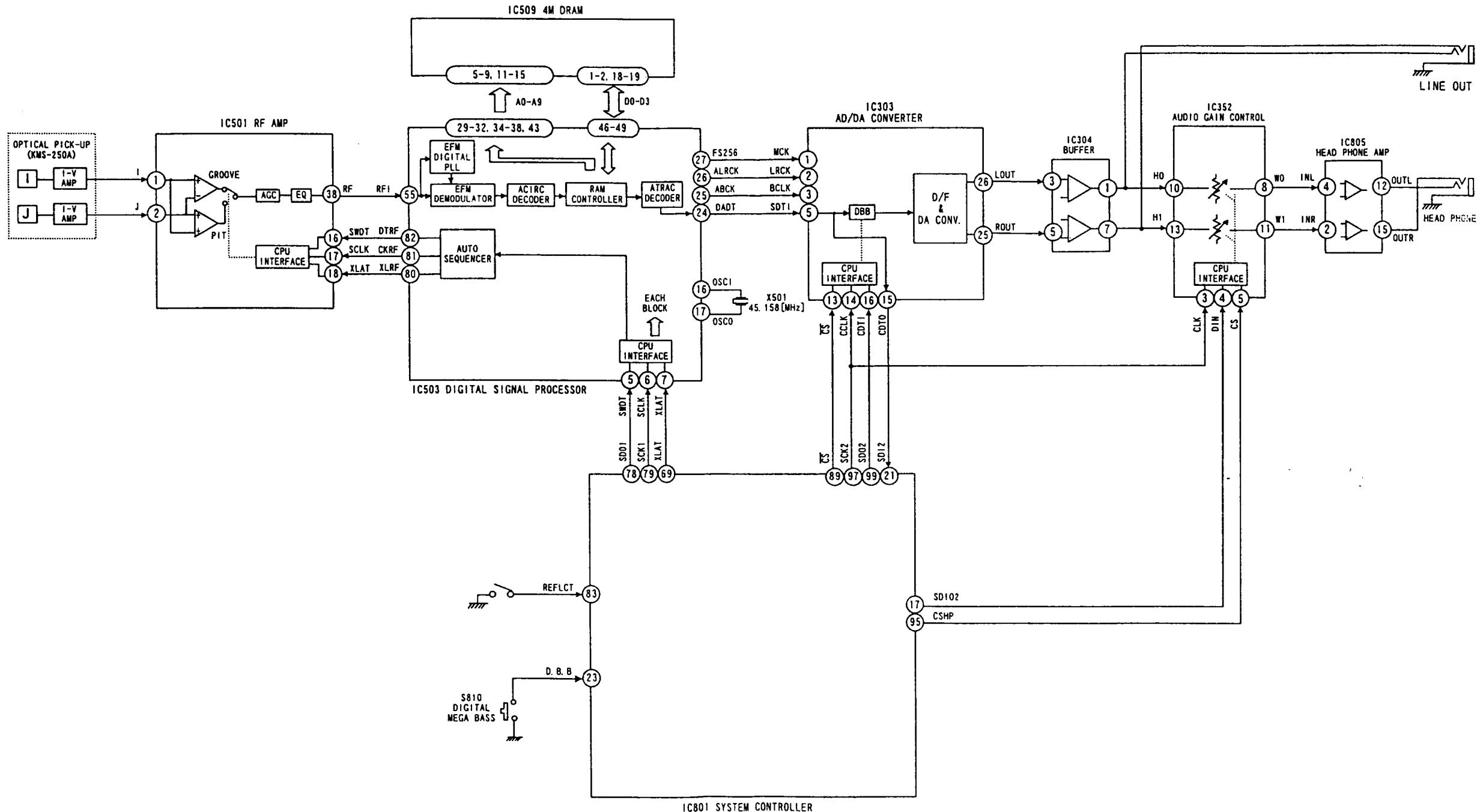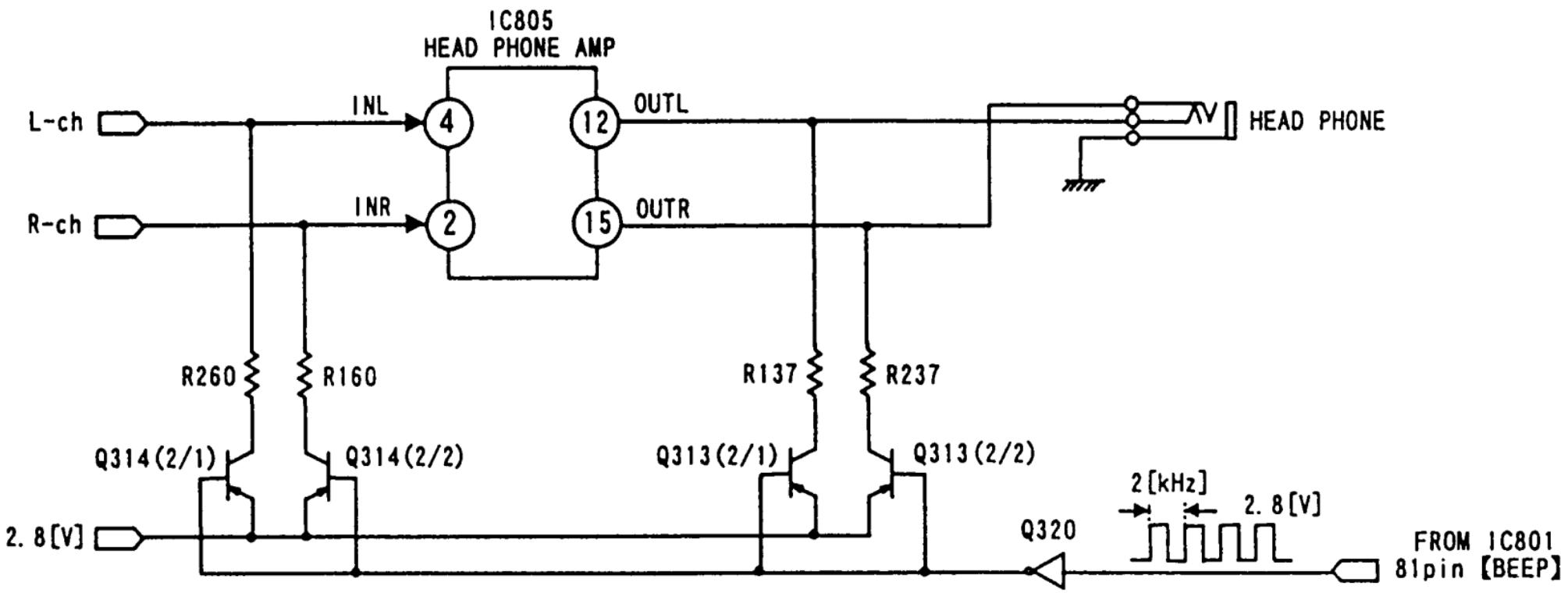
Fig. 6-5 BEEP Generation Circuit

IC801
81pin 【BEEP】

2. 8 [V]

0

0. 4 [s]   1. 15 [s]
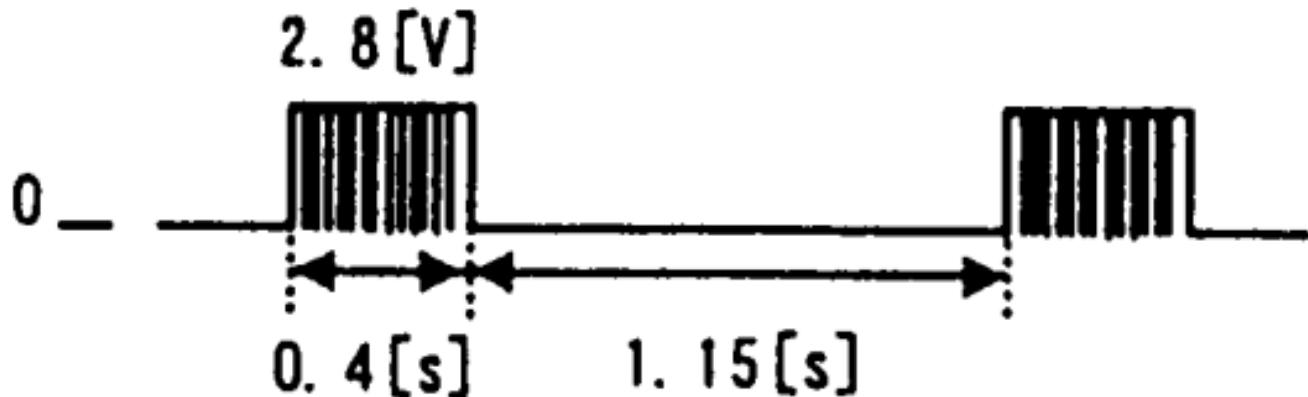
Fig. 6-6 BEEP Output (During Pause)
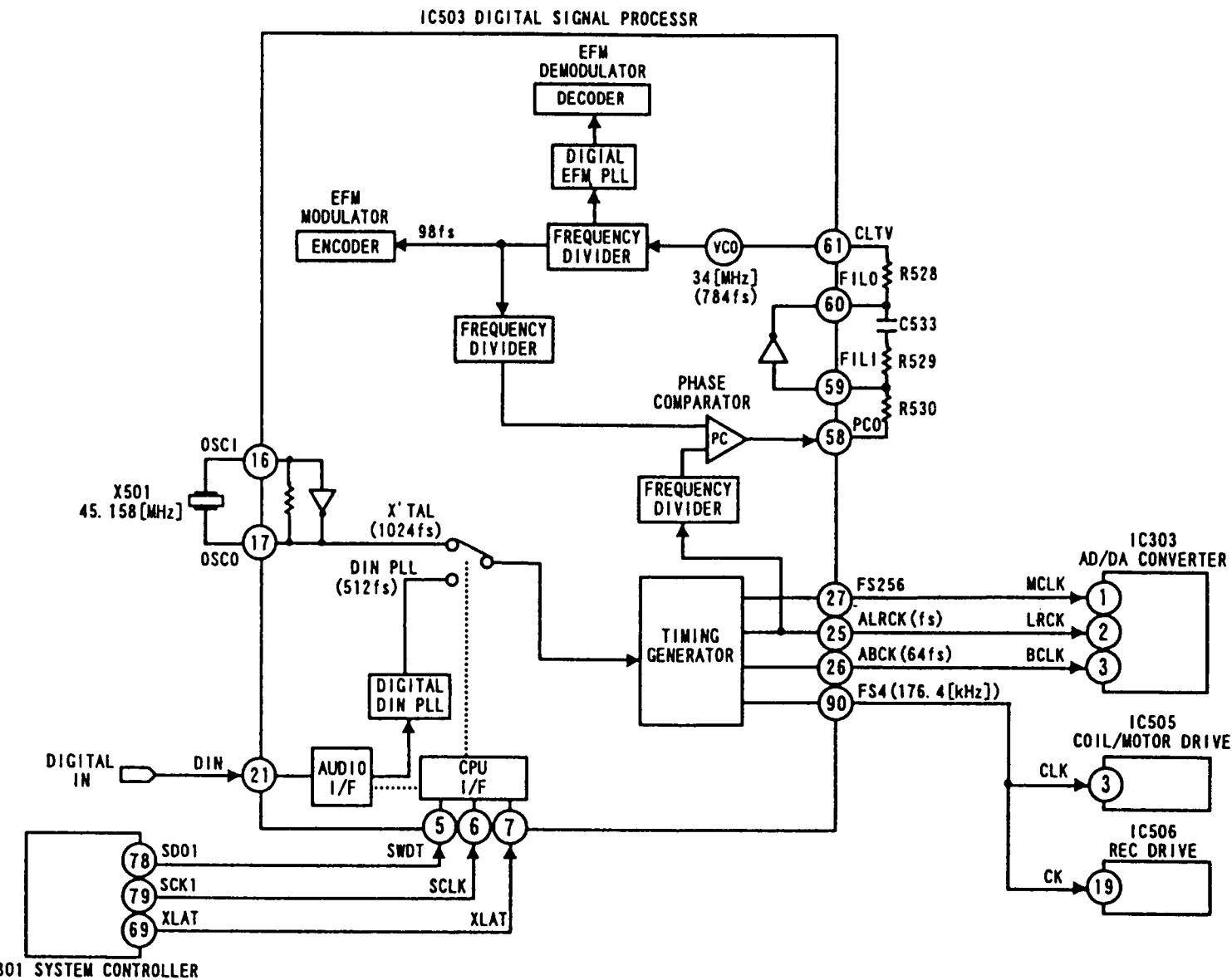
Fig. 6-7 PLL Circuit and Clock System

Table. 6-5 Operation Modes of PLL Circuit

MODE	Reference Oscillator	Operation PLL	Purpose
Analog recording	X501　　　　　: 1024 fs	Encoder PLL	Generation of channel clock for EFM modulation
Digital recording	Digital IN PLL　: 512 fs	Digital IN PLL → Encoder PLL	Generation of channel clock for EFM modulation
Playback	X501　　　　　: 1024 fs	Decoder digital PLL	Generation of channel clock for EFM demodulation
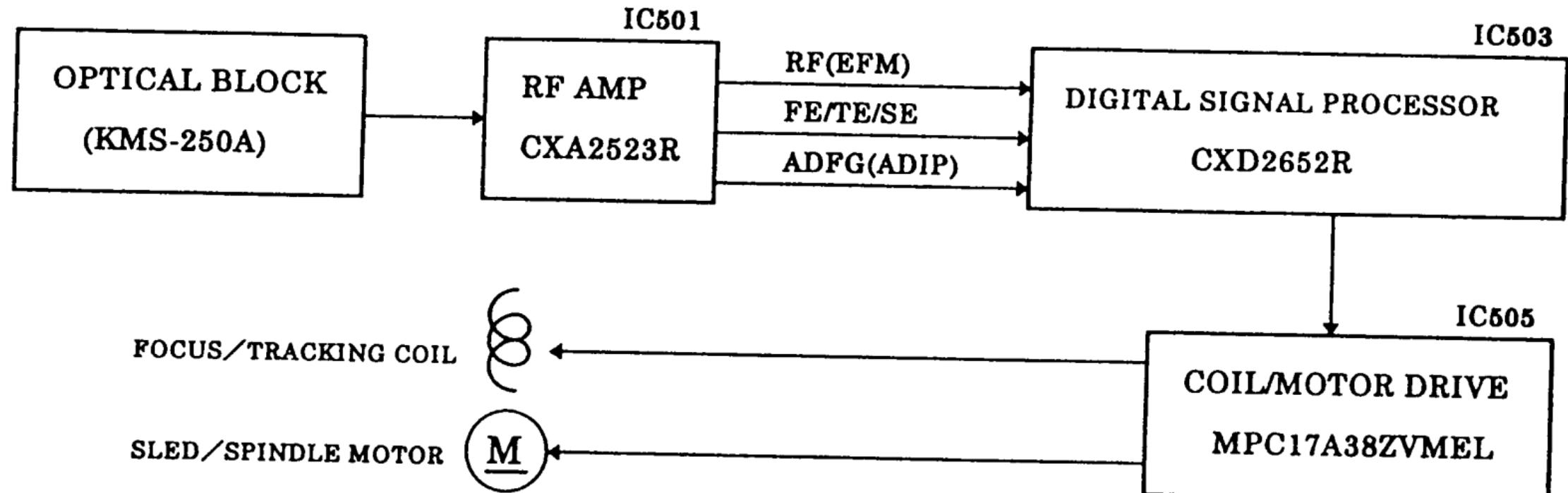
Fig. 7-1 Block Diagram of Servo Circuit
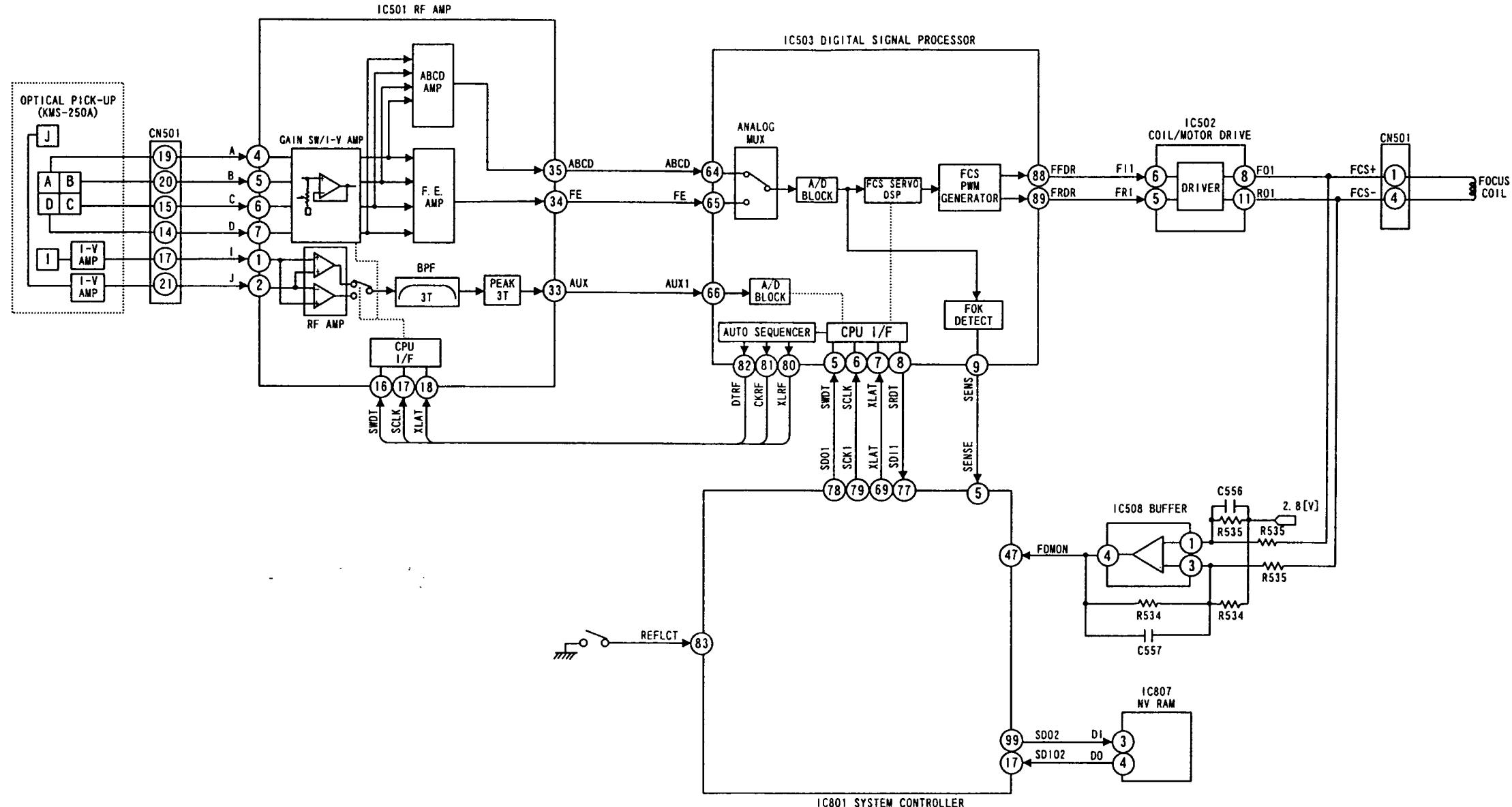
Fig. 7-2 Focus Servo Circuit
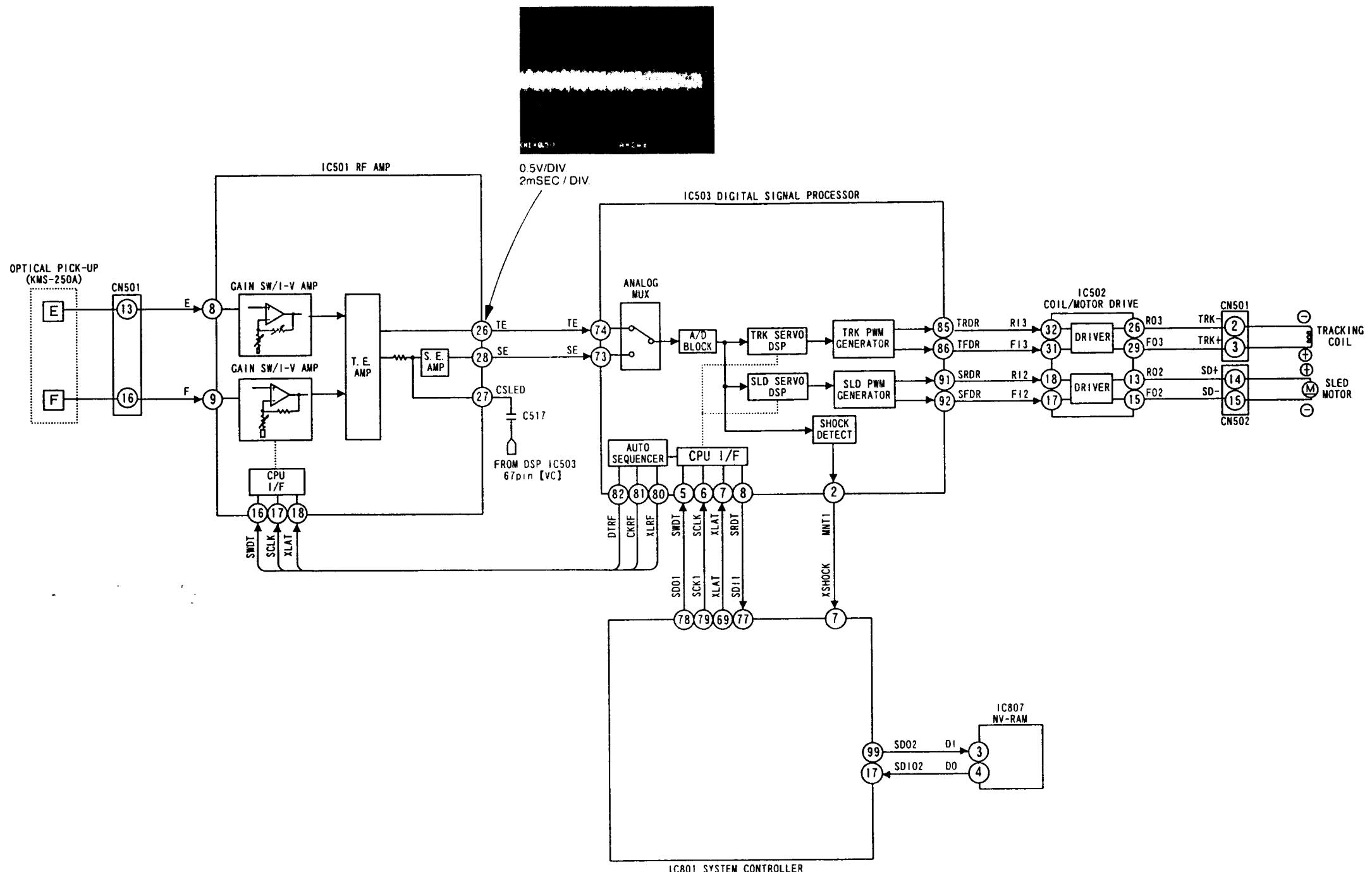
Fig. 7-3 Tracking/Sled Servo Circuit

Table. 7-1 Spindle Servo Mode

Disc Type	Recorded side	Servo mode
MO groove	Groove	ADIP-CLV
MO pit (PTOC)	Pit	EFM-CLV
CD pit	Pit	EFM-CLV

Table. 7-2 CLV Mode

Mode	Details		
CLVS	Rough servo for fetching		
CLVP	PLL mode		
CLVA	Auto mode	Checks GFS when EFM-CLV[7-1]	"H" → CLVP, "L" → CLVS
		Checks CRC when ADIP-CLV	"OK" → CLVP, "NG" → CLVS
CLVH	Rough servo in high speed access		

*7-1. GFS becomes "H" when the frame sync played back obtained at the correct timing.
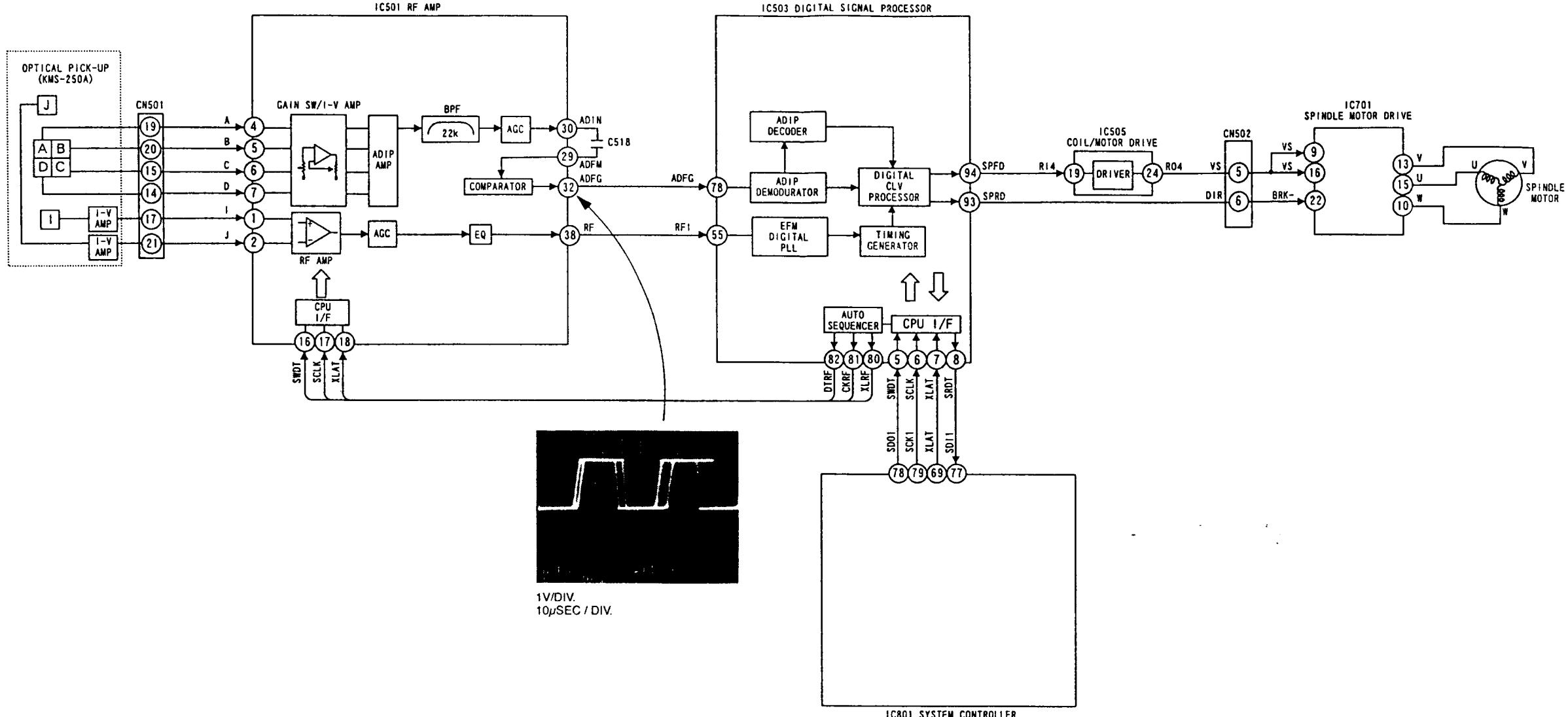
Fig. 7-4 Spindle Servo Circuit
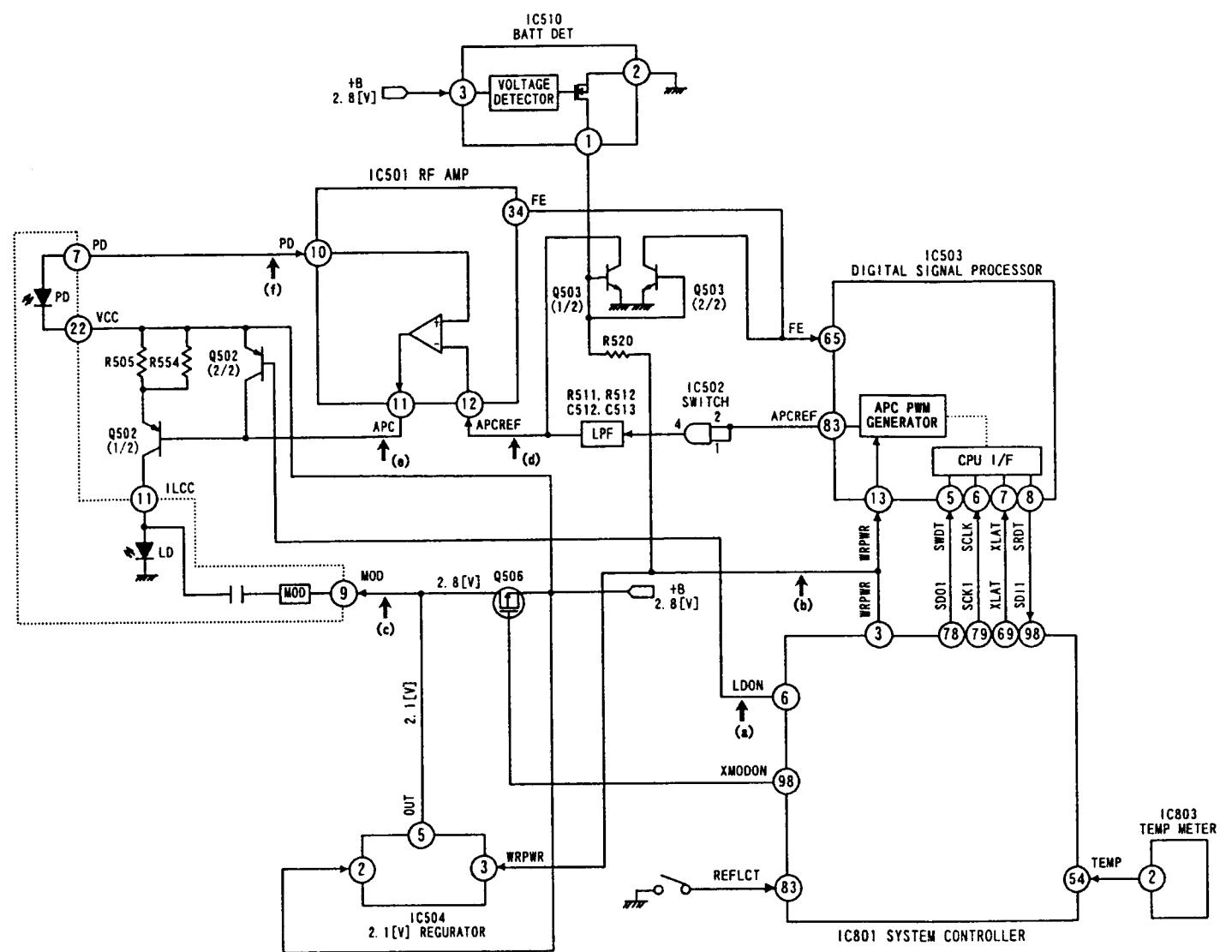
Fig. 8-1 APC and Laser Power Circuit

(A) When the battery is running

(B) When the DC power supply is running

Fig. 8-1 APC and Laser Power Circuit

(A) When the battery is running
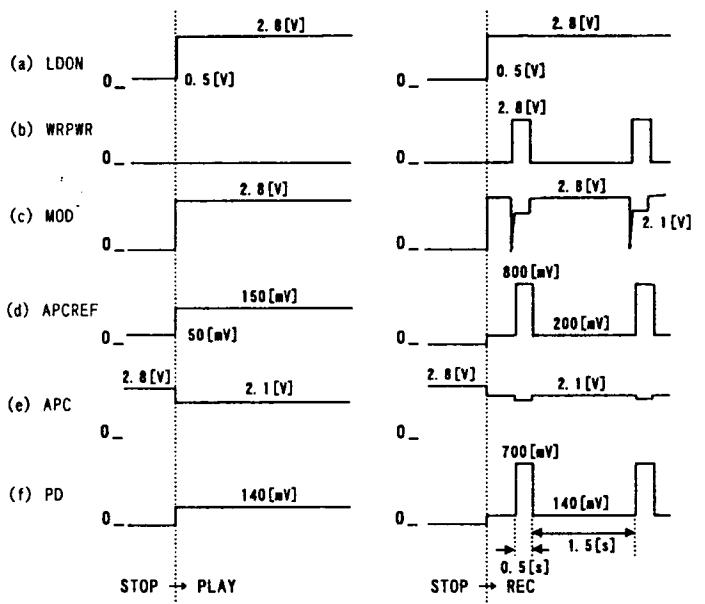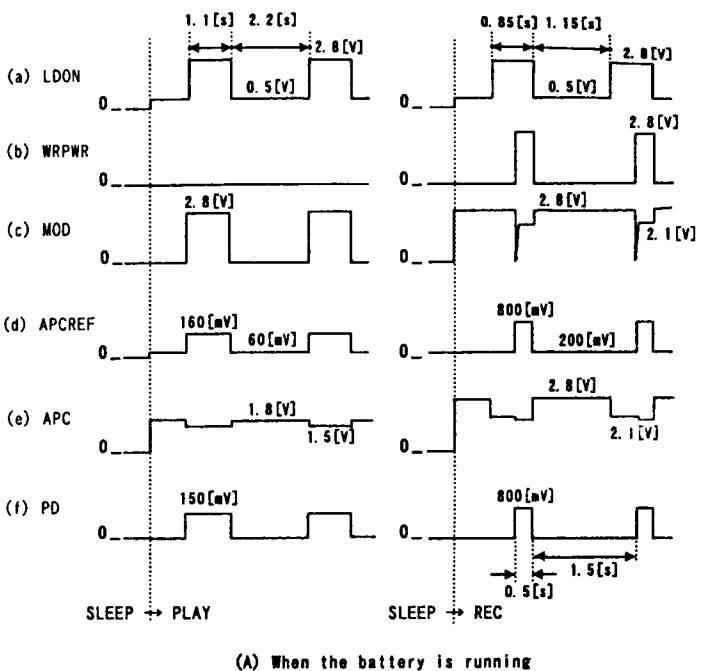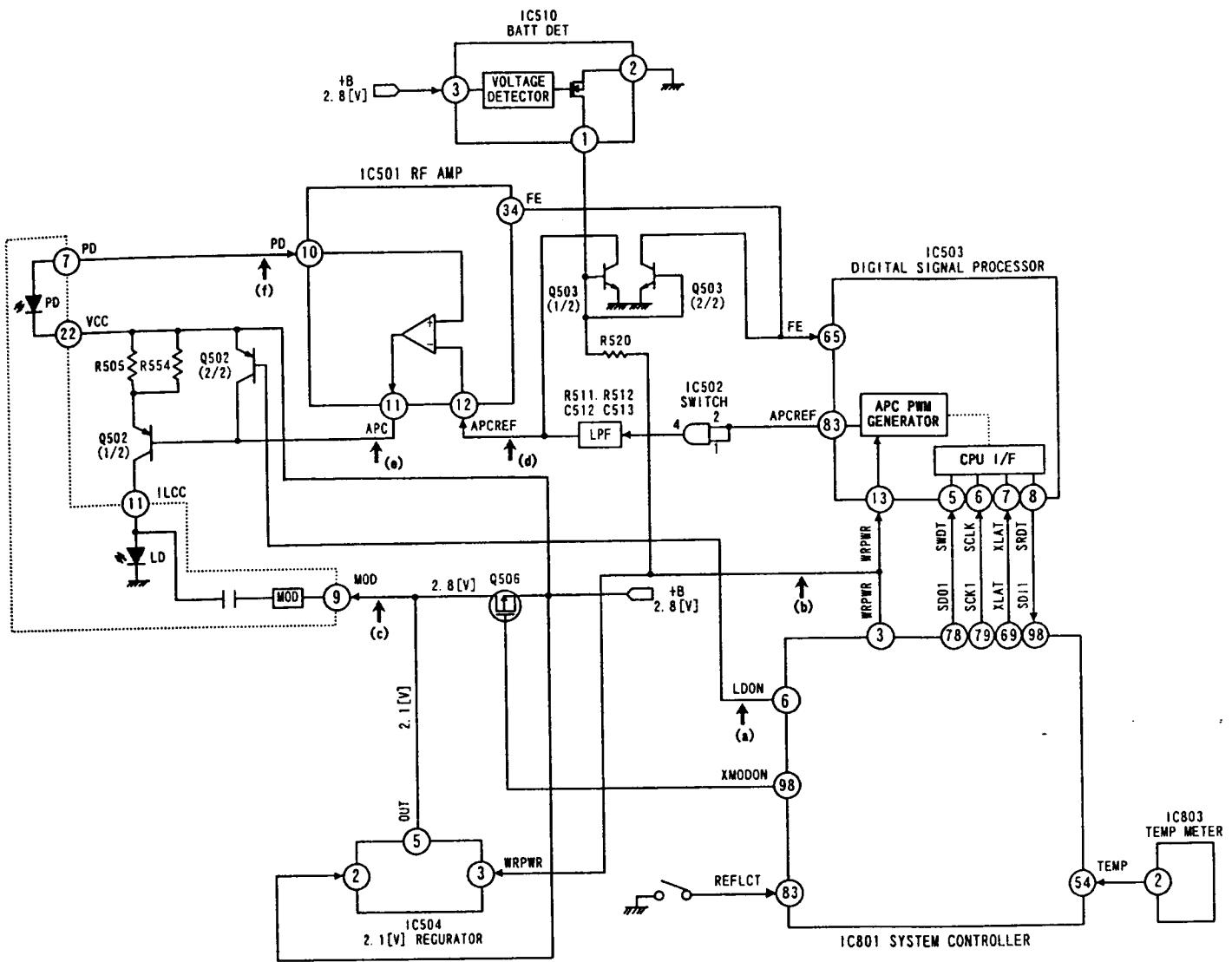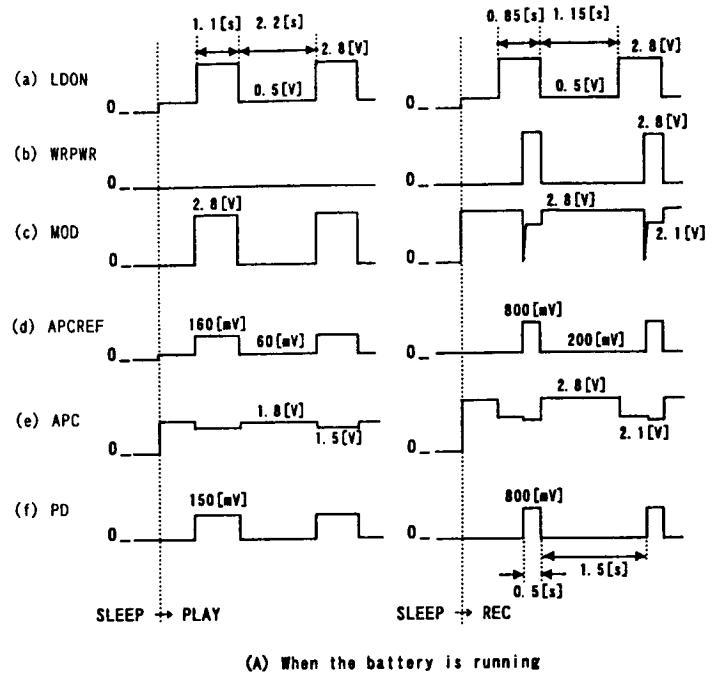
(B) When the DC power supply is running
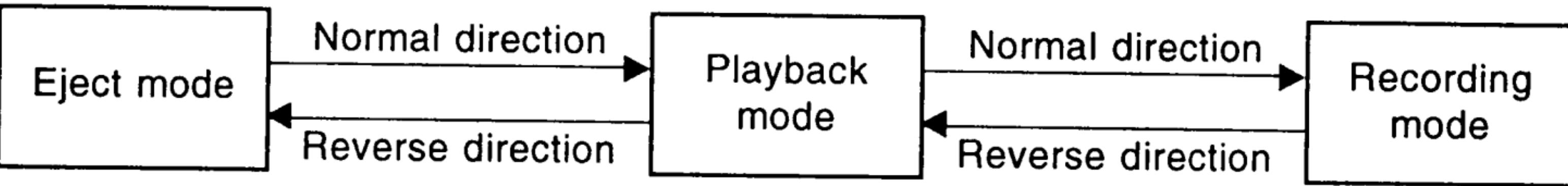
Fig. 9-1 Change in Mechanism Mode

9-3. Change in Mechanism Mode

(A) REAR SIDE OF MECHANISM DECK

(B) UPPER SIDE OF MECHANISM DECK
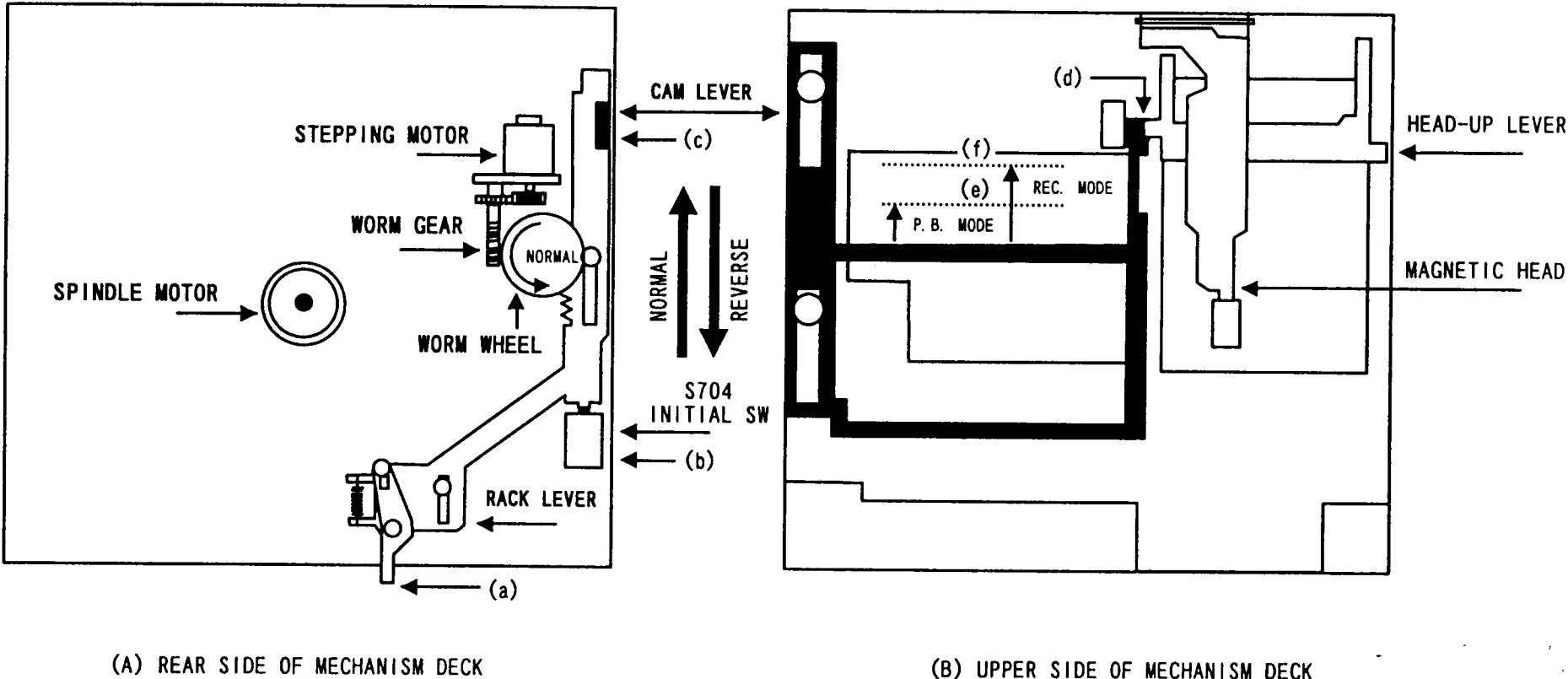
Fig. 9-2 Change in Mechanism Operations

9-4. Stepping Motor Control Circuit
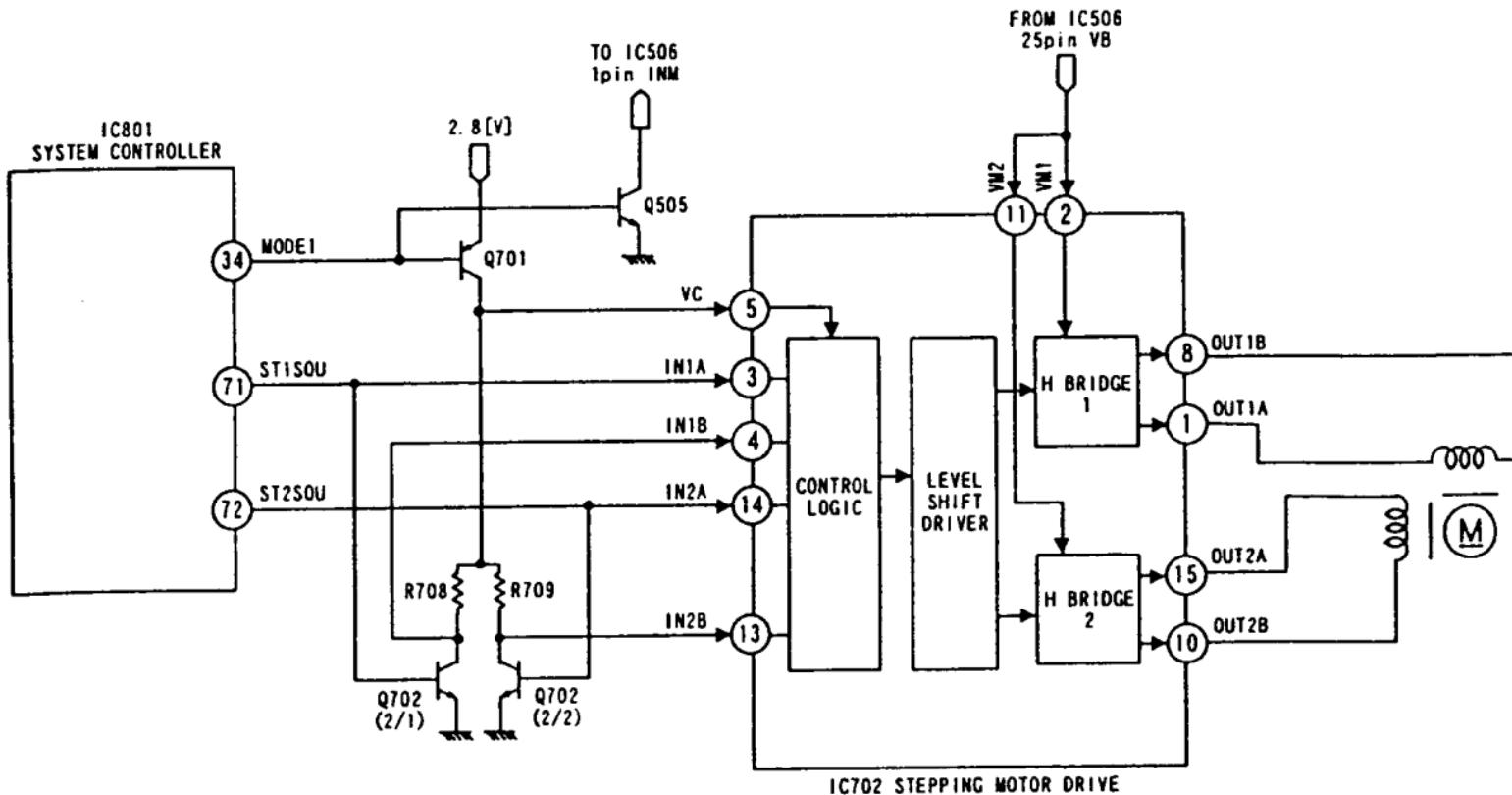
Fig. 9-3 Stepping Motor Control Circuit

Table. 9-1 Stepping Motor Driver Inputs/Outputs

IN1A (IN2A)	IN1B (IN2B)	OUT1A (IN2A)	OUT1B (IN2B)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	Z	Z

IC801
71pin [ST1SOU]

7.75[ms]

3.2[V]

0

IC801
72pin [ST2SOU]

3.2[V]

0
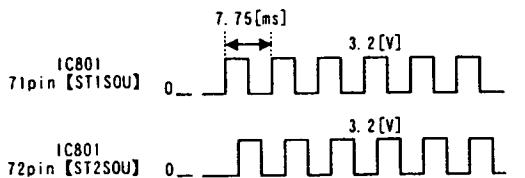
(A) Operation when the stepping motor is driven
in the normal direction

IC801
71pin [ST1SOU]

7.75[ms]

3.2[V]

0

IC801
72pin [ST2SOU]

3.2[V]

0
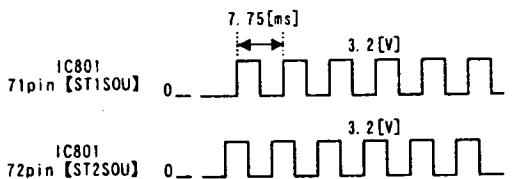
(B) Operation when the stepping motor is driven
in the reverse direction

IC801
64pin [INTSW]

3.2[V]

0

IC801
71pin [ST1SOU]

290[ms]

3.2[V]

0

IC801
72pin [ST2SOU]

3.2[V]

0

(C) STOP → PLAY

IC801
64pin [INTSW]

3.2[V]

0

IC801
71pin [ST1SOU]

440[ms]

3.2[V]

0

IC801
72pin [ST2SOU]

3.2[V]

0

(D) PLAY → STOP

IC801
64pin [INTSW]

3.2[V]

0

IC801
71pin [ST1SOU]

697[ms]

3.2[V]

0

IC801
72pin [ST2SOU]

3.2[V]

0

(E) STOP → REC

IC801
64pin [INTSW]

3.2[V]

0

IC801
71pin [ST1SOU]

943[ms]

3.2[V]

0

IC801
72pin [ST2SOU]

3.2[V]

0
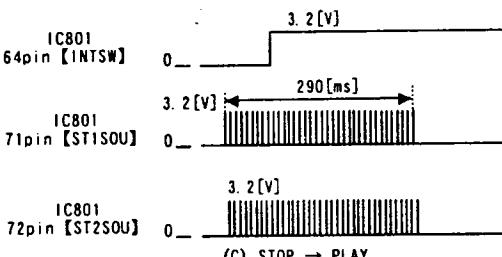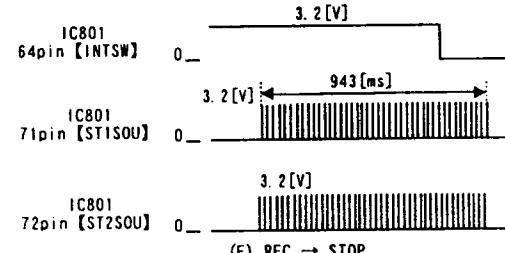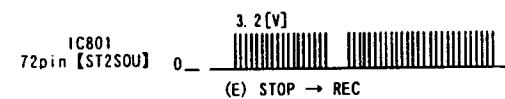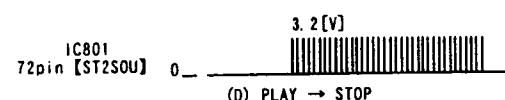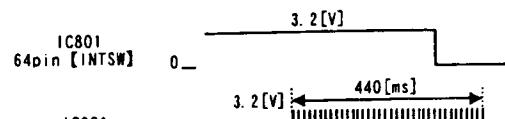
(F) REC → STOP

Fig. 9-4 Waveform Timing during Operations